High Throughput Secure MPC Over Small Population in Hybrid Networks

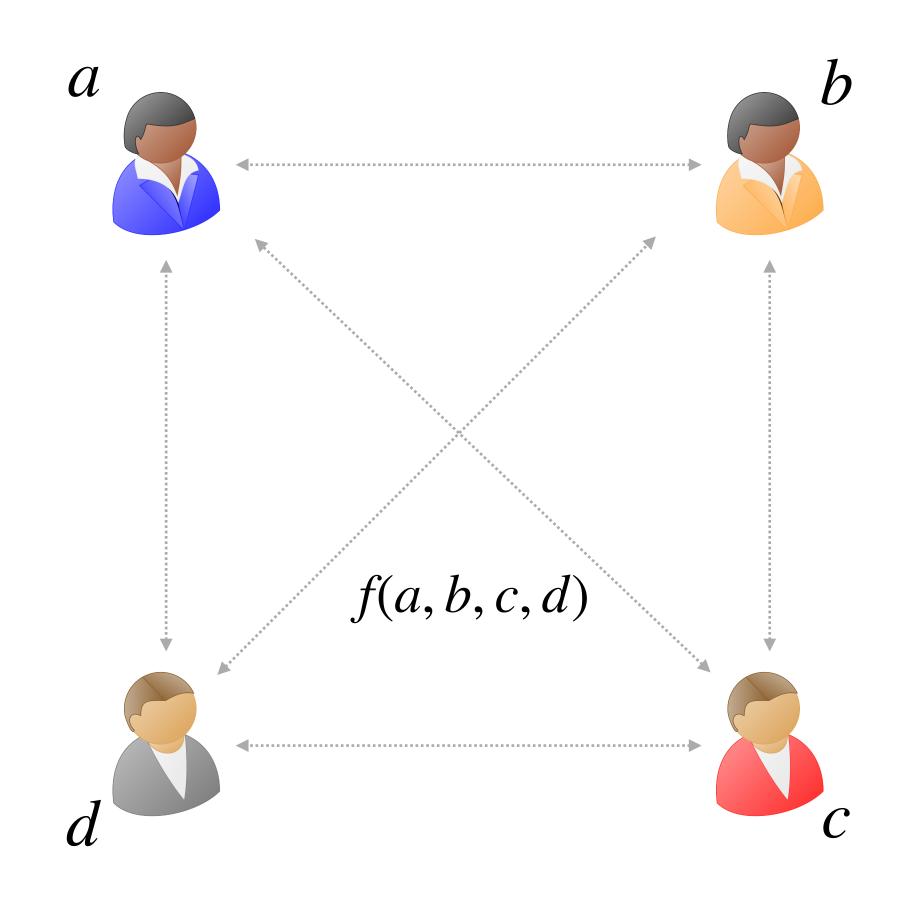
Ashish Choudhury, <u>Aditya Hegde</u>



INDOCRYPT 2020



Distrusting parties compute a function on • private inputs



- Distrusting parties compute a function on • private inputs
- Equivalent to interacting with a Trusted Third Party (TTP)



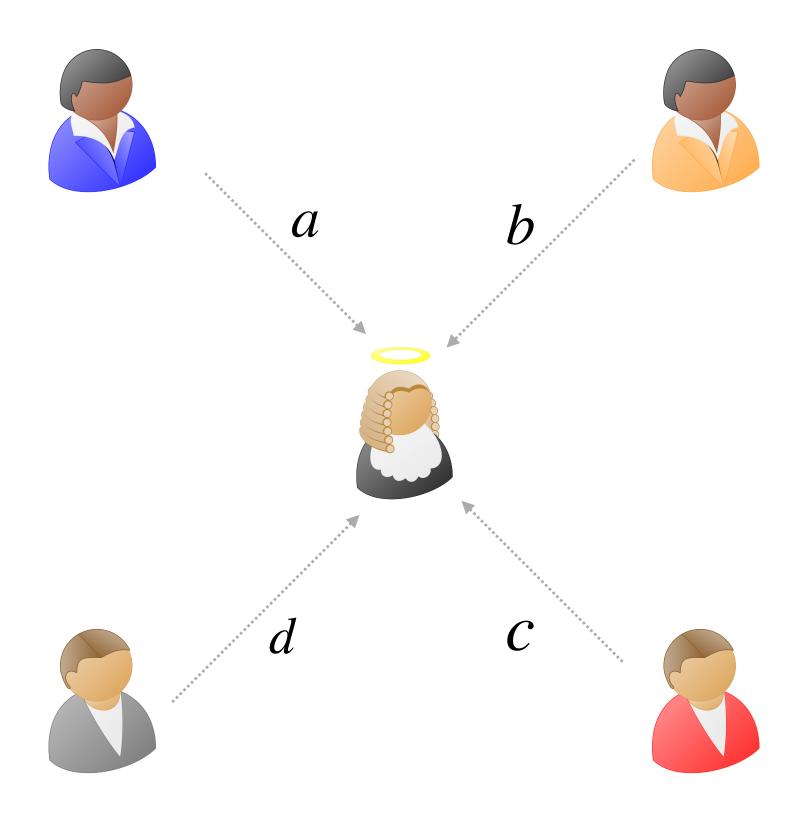




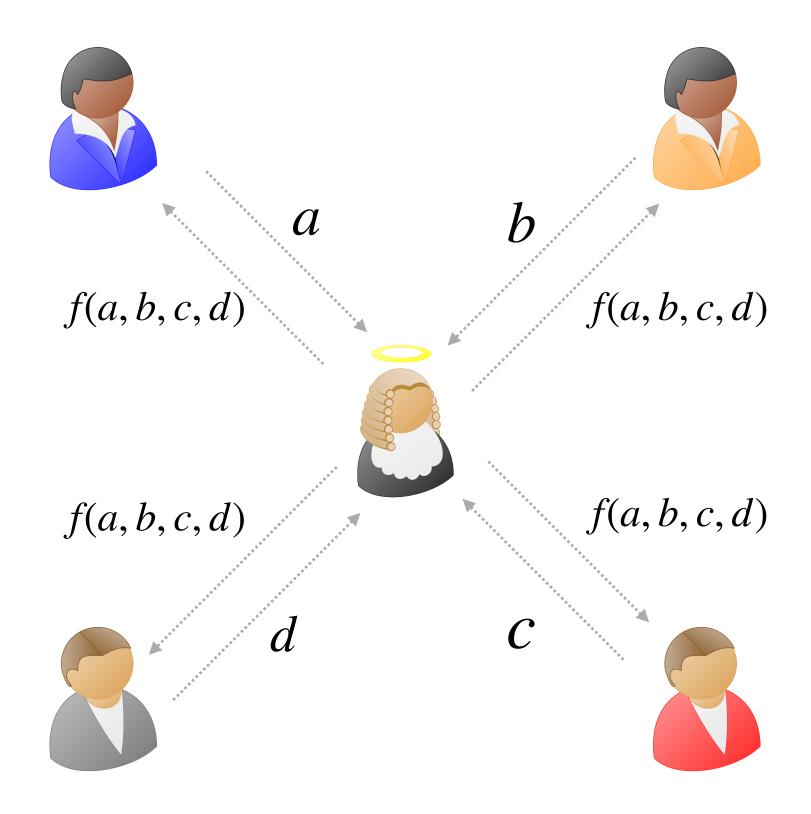




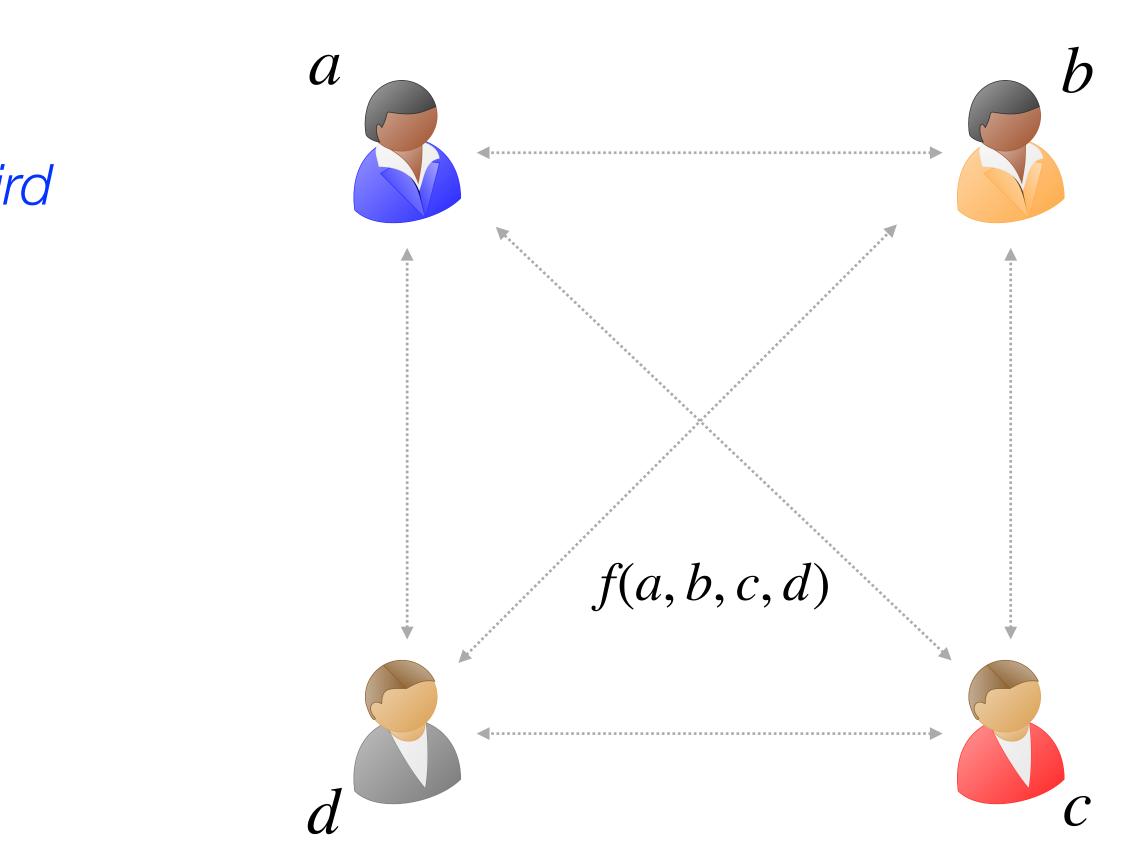
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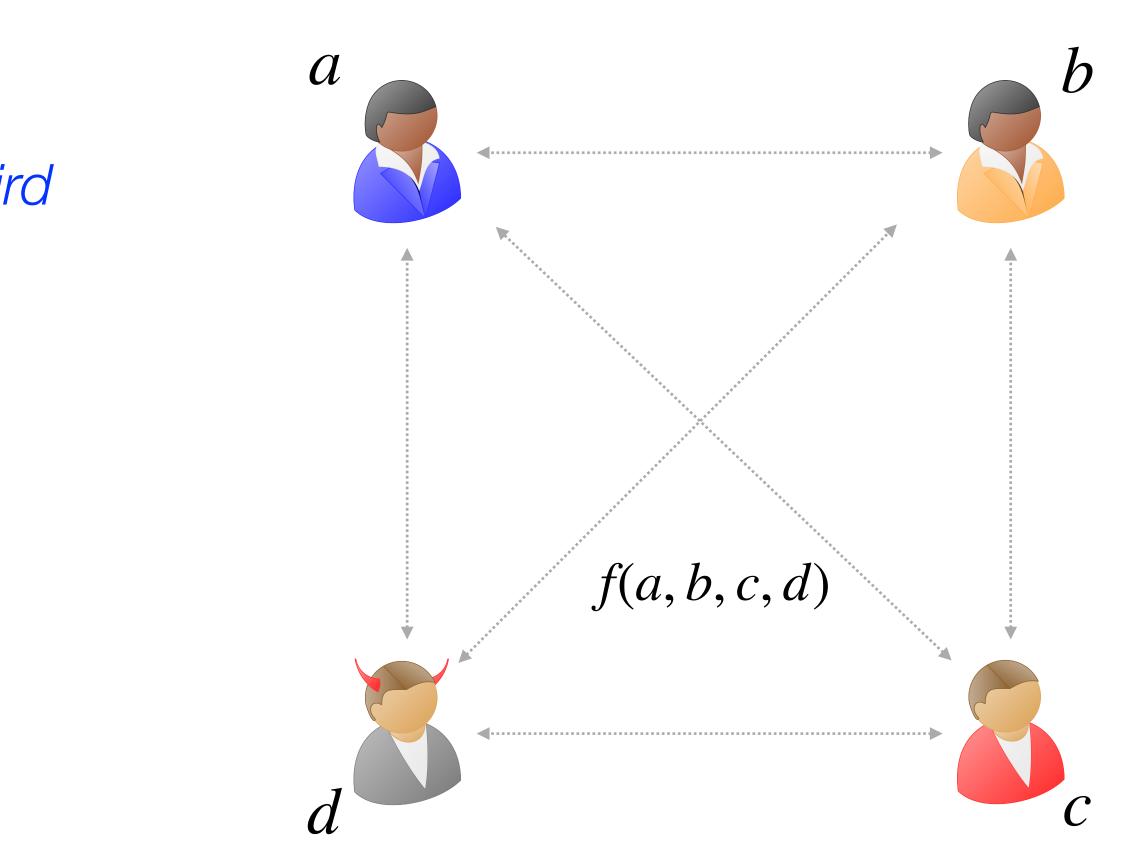
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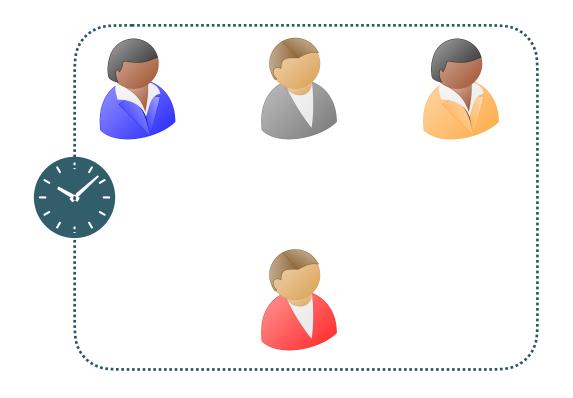


- Distrusting parties compute a function on • private inputs
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 - Simple and efficient \implies Practical applications
- Setting •
 - n = 4, t = 1
 - Malicious adversary

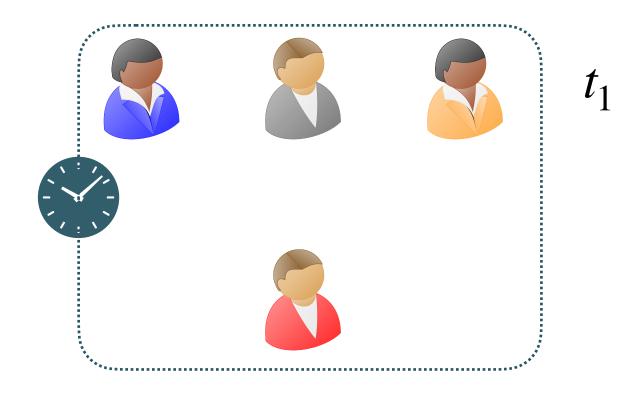


• Pairwise private and authentic channels

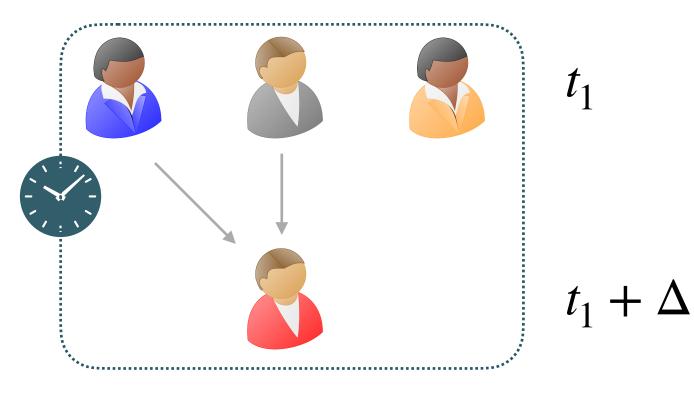
- Pairwise private and authentic channels •
- Synchronous networks
 - Global clock •
 - Publicly known upper bound on message delay



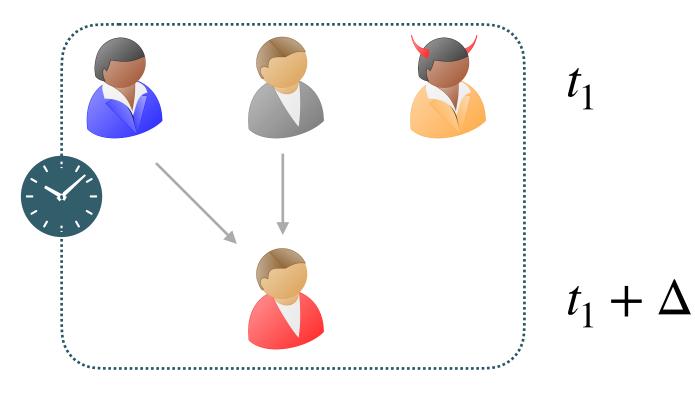
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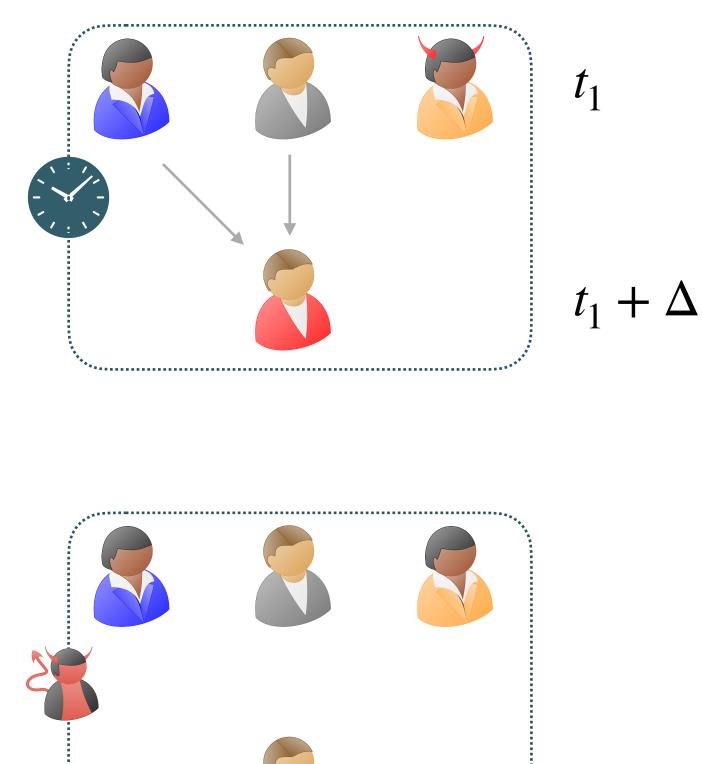
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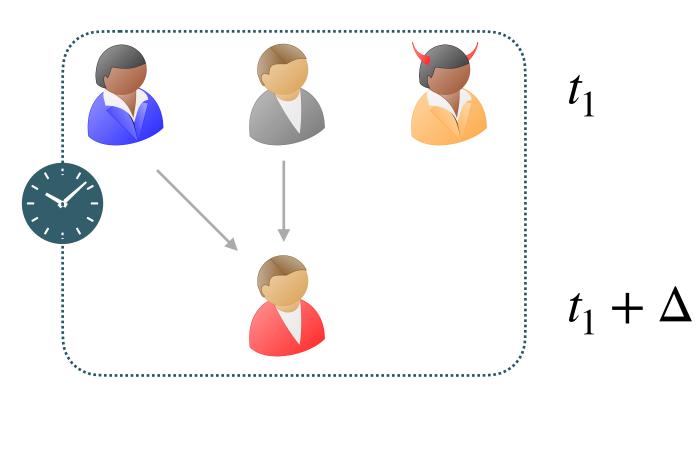
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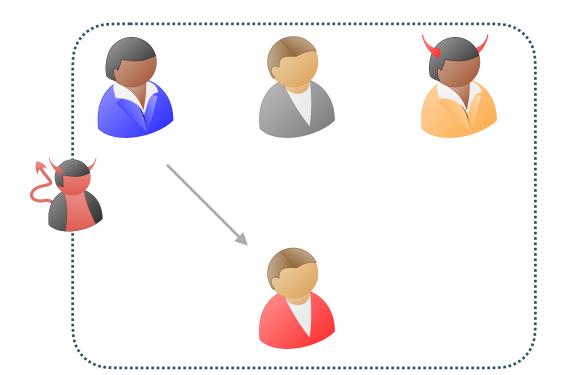


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- Asynchronous networks [BCG93,Canetti95] •
 - No synchronisation •
 - Adversary schedules messages •
 - Eventual delivery



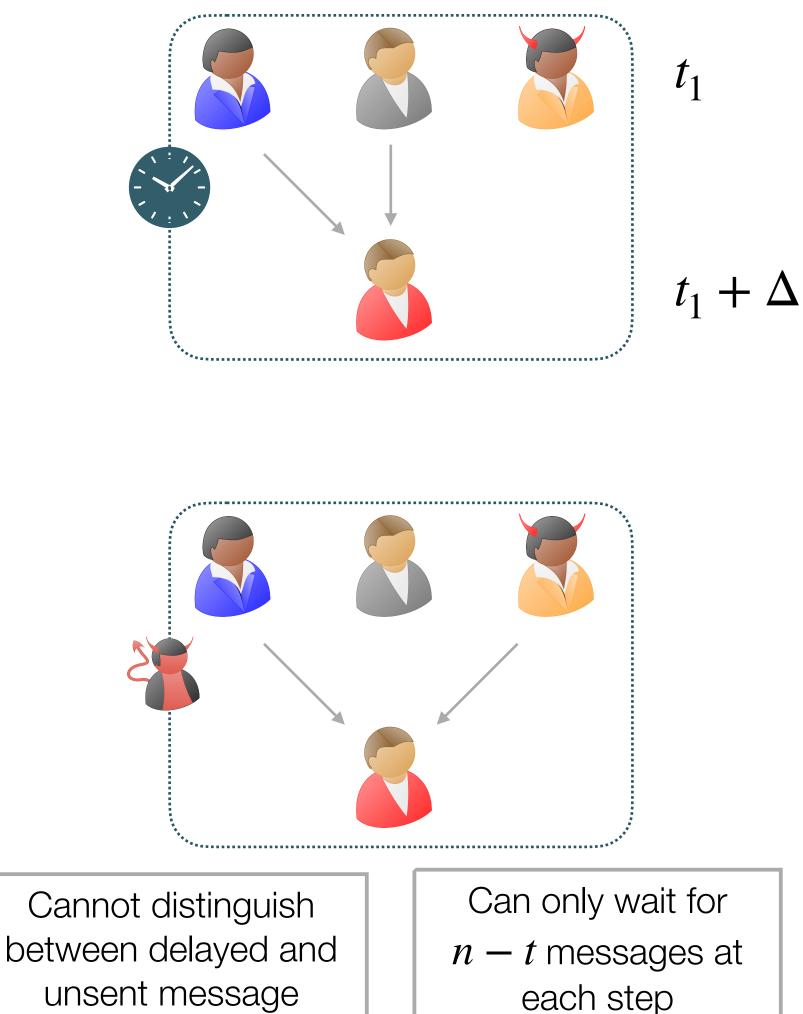
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Cannot distinguish between delayed and unsent message

- Pairwise private and authentic channels •
- Synchronous networks •
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Communication Model - Hybrid Networks

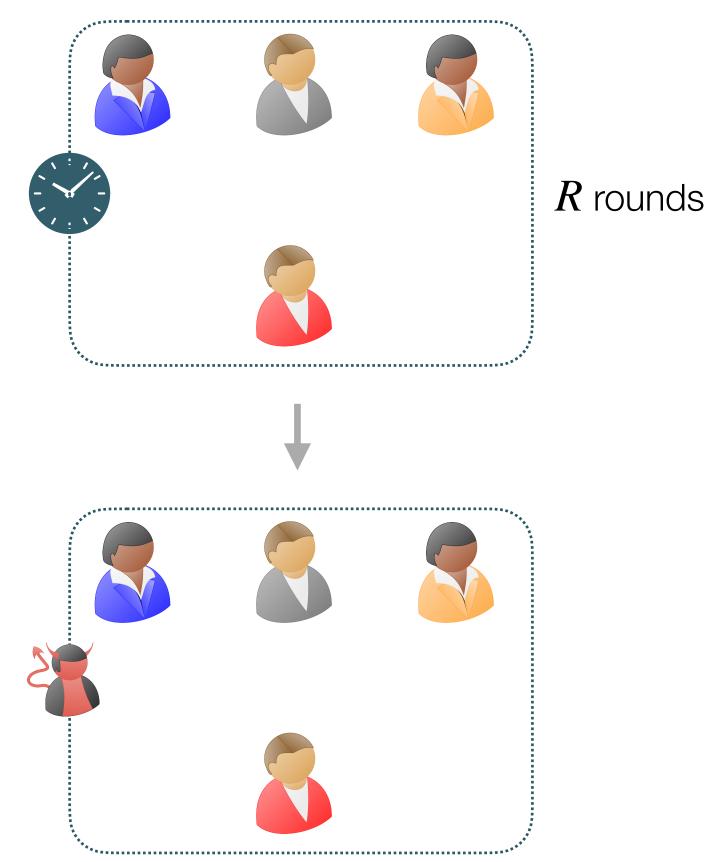
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- **Hybrid networks**: *R* initial synchronous rounds followed by • asynchronous computation [BHN10,CHP13,PR18]
 - Assume synchronous broadcast channel in first Rrounds

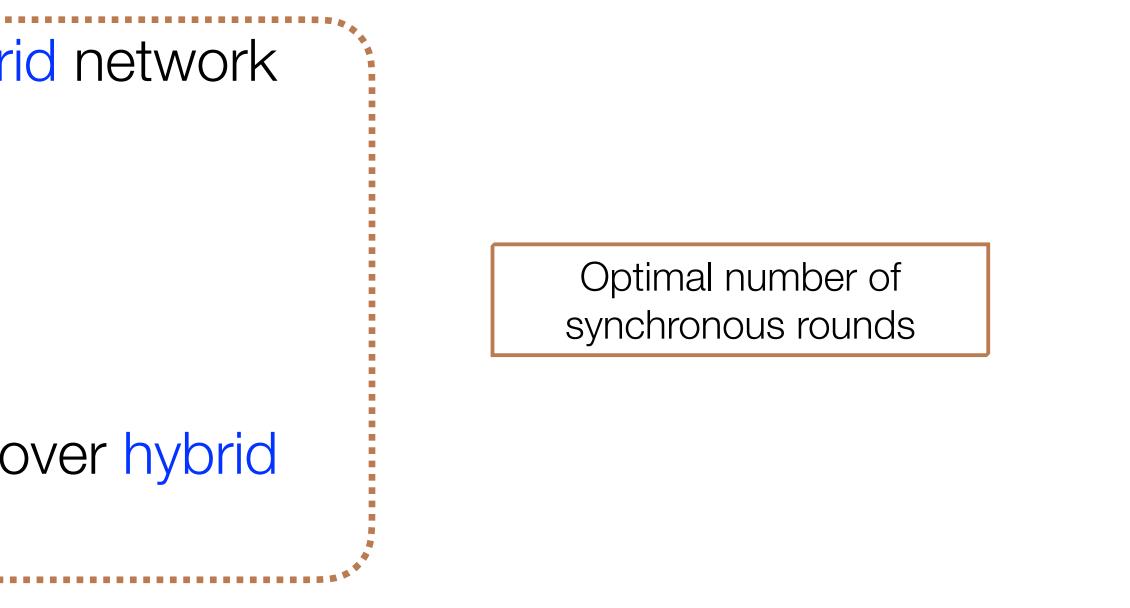


- Perfectly secure MPC protocol over hybrid network with R = 2
 - First protocol in this setting
- Cryptographically secure MPC protocol over hybrid network with R = 1
- Cryptographically secure MPC protocol over asynchronous network

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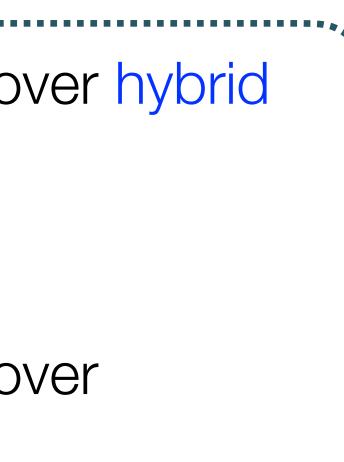


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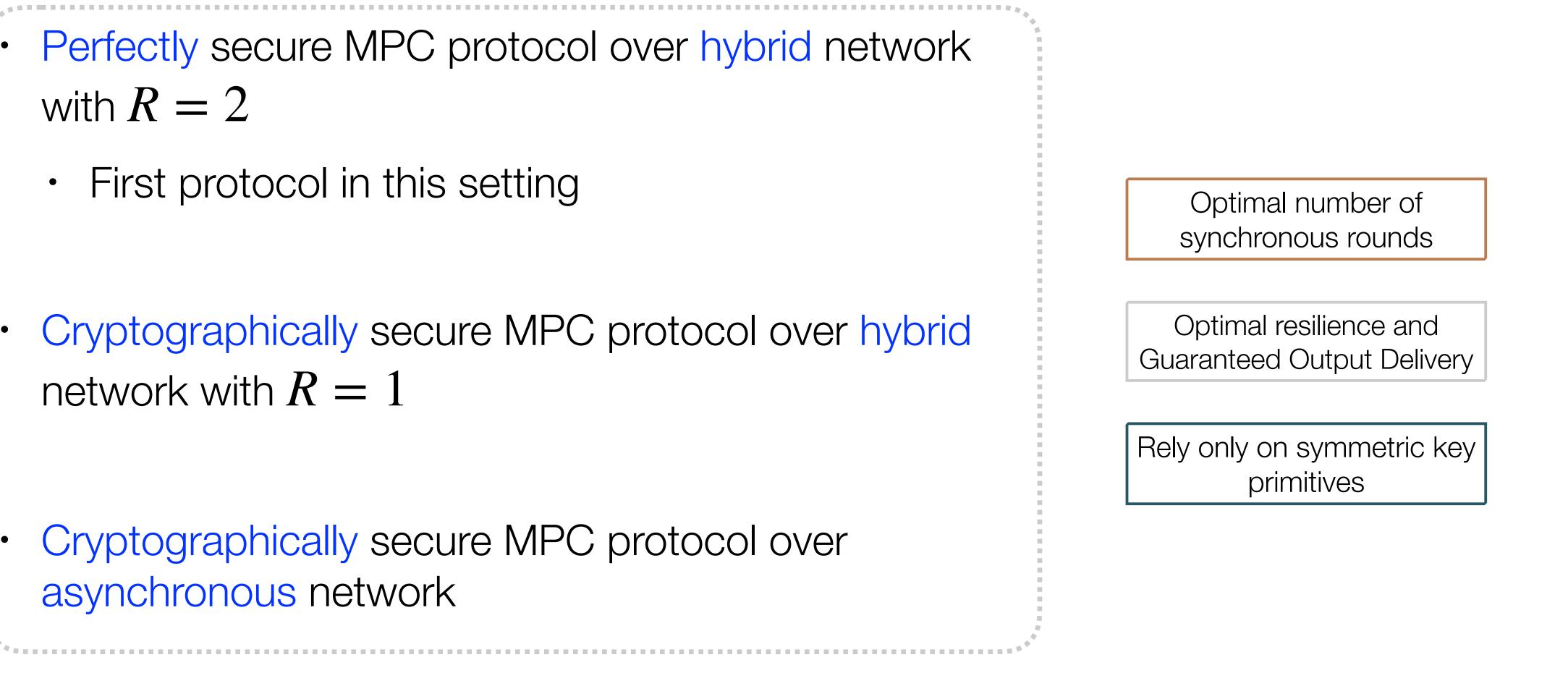




Optimal number of synchronous rounds

Rely only on symmetric key primitives

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 - Implementation and benchmarks

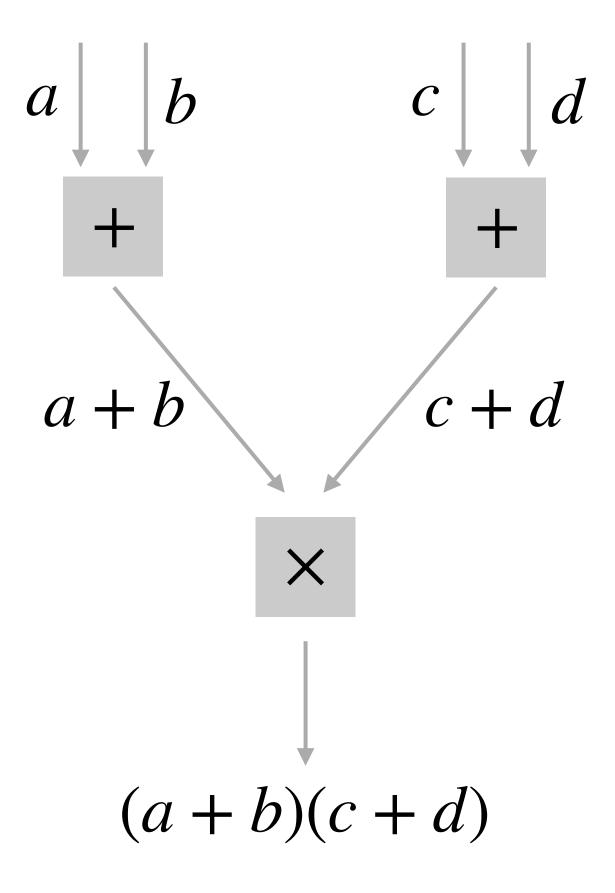
Optimal resilience and Guaranteed Output Delivery

Optimal number of

synchronous rounds

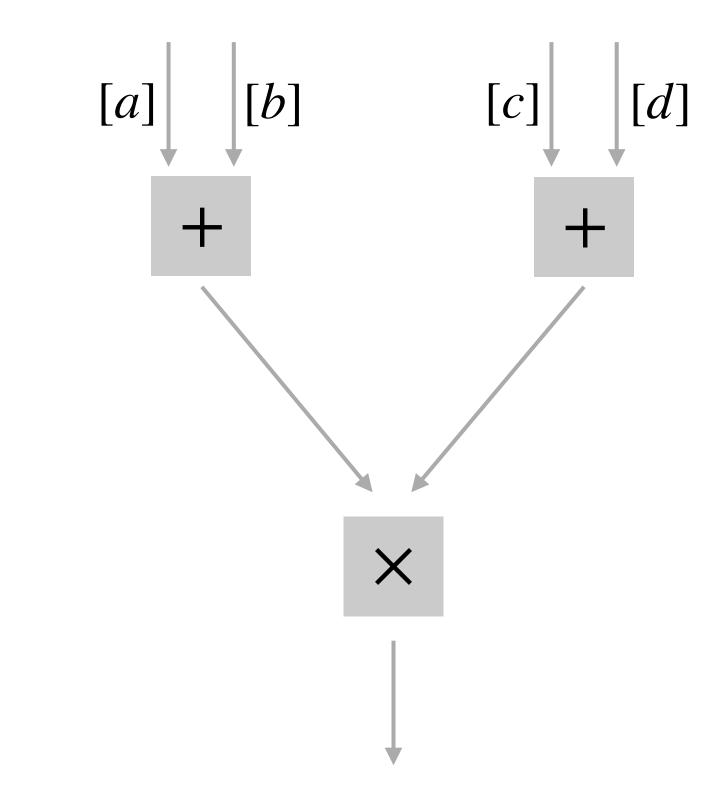
Rely only on symmetric key primitives

• *f* represented as arithmetic circuit over finite field



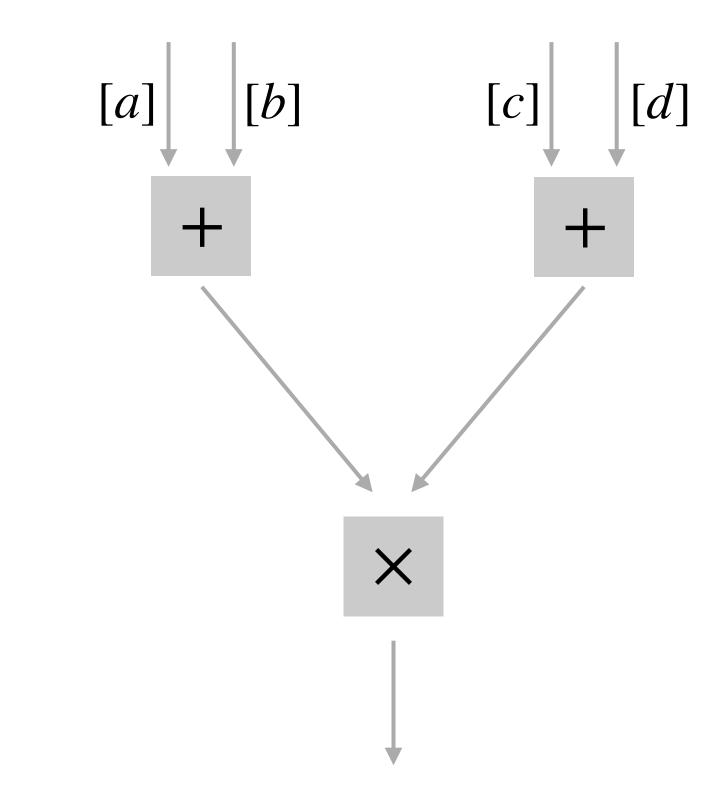
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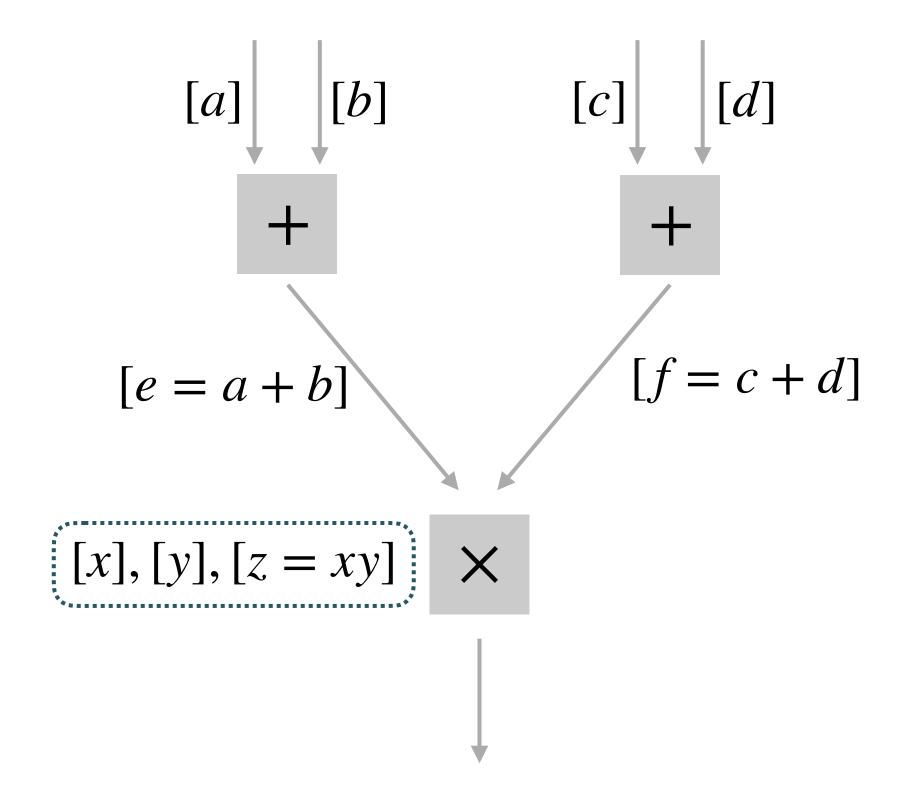
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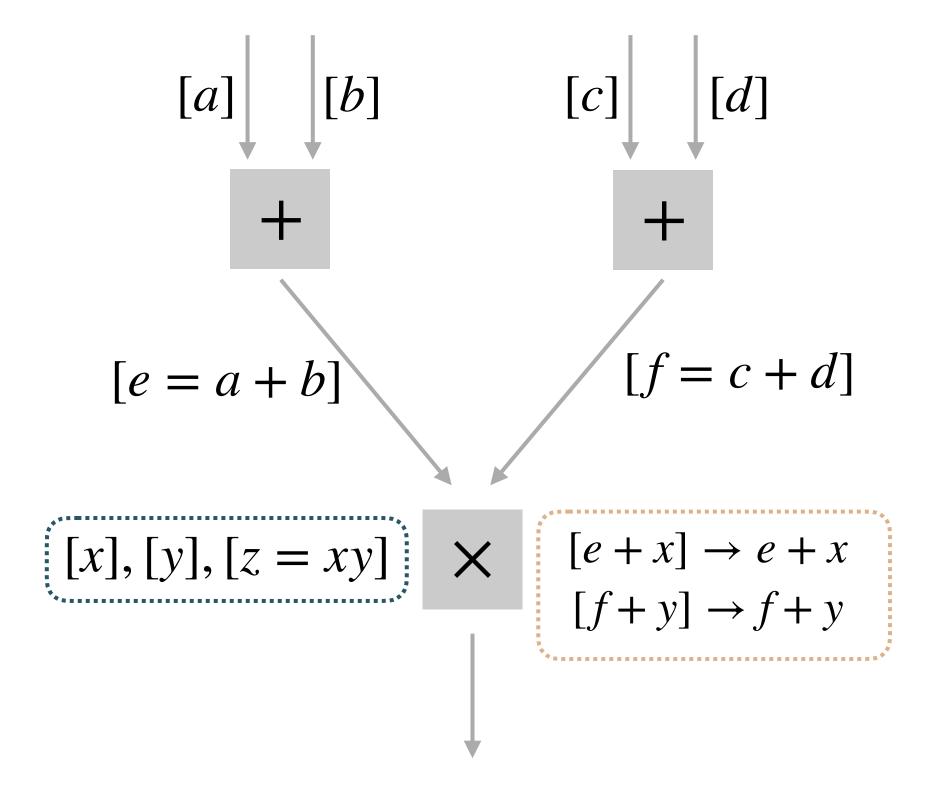
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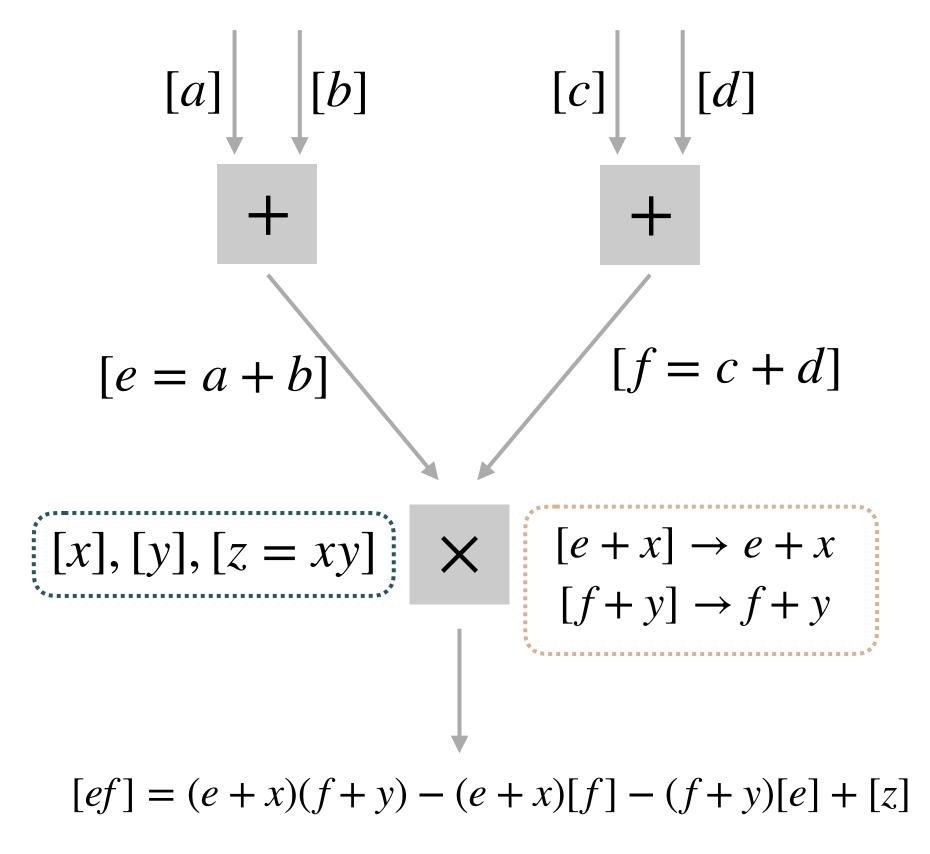


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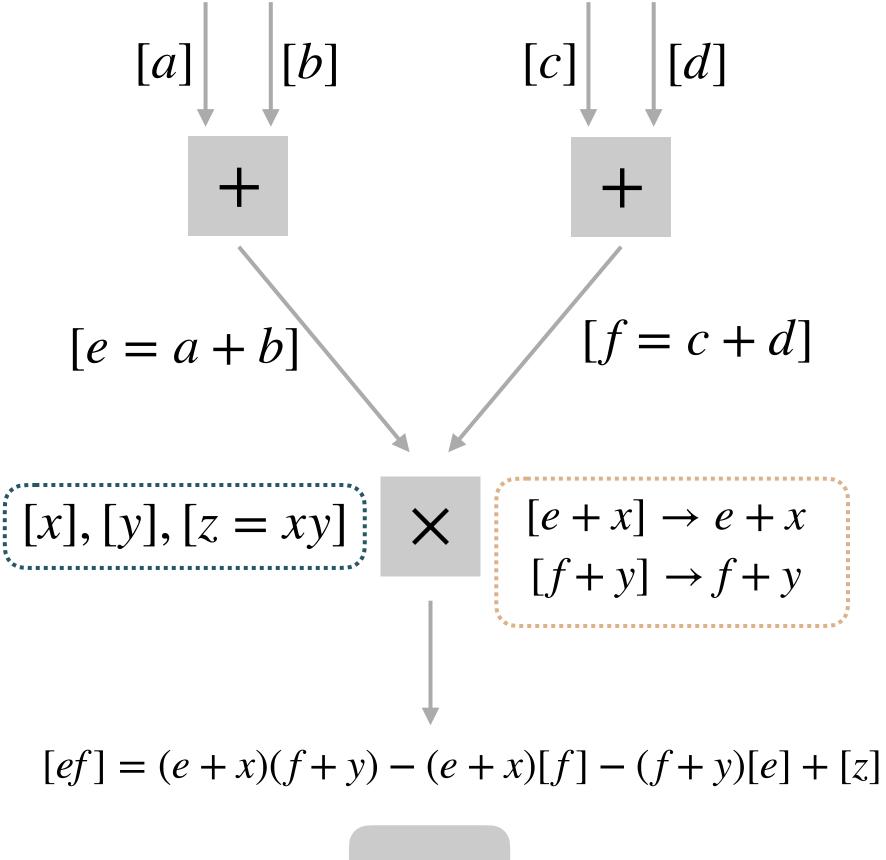


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Beaver

Triple generation framework of [CP17]



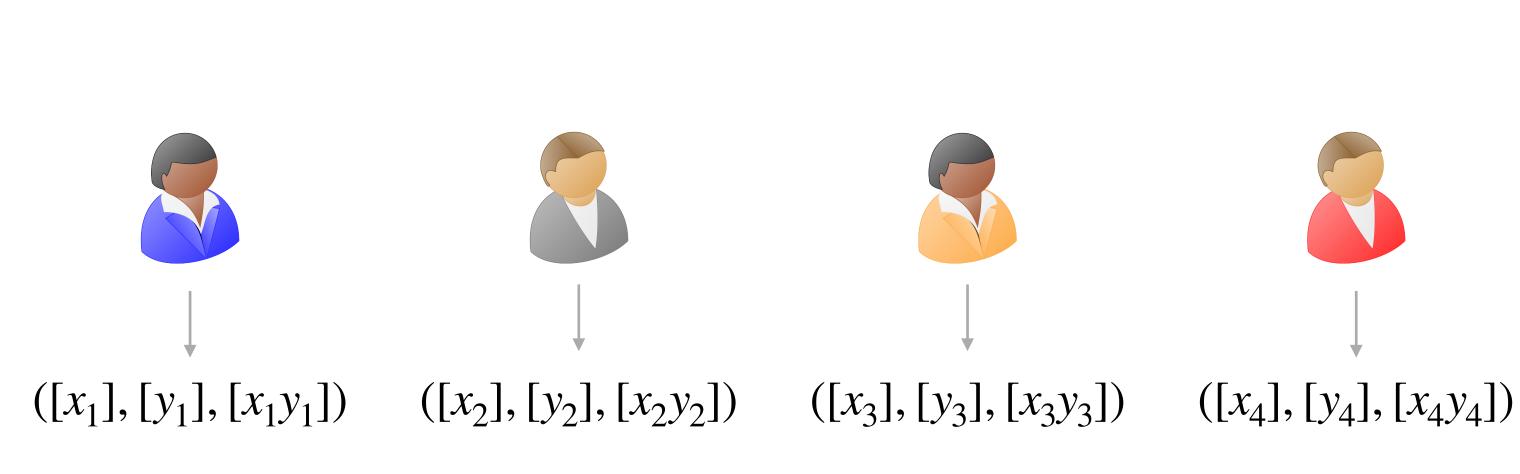




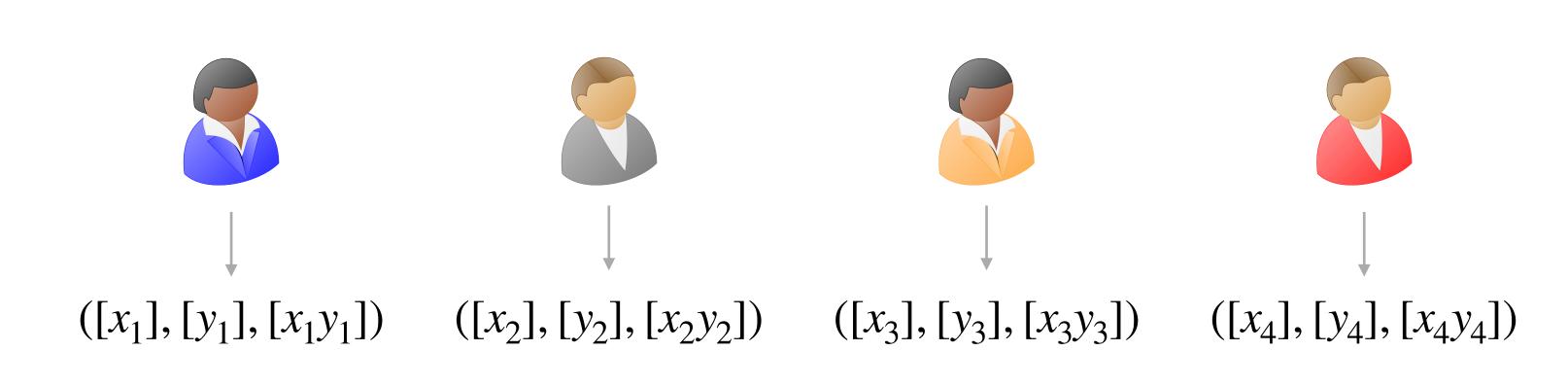




- Triple generation framework of [CP17]
 - Triple sharing protocol



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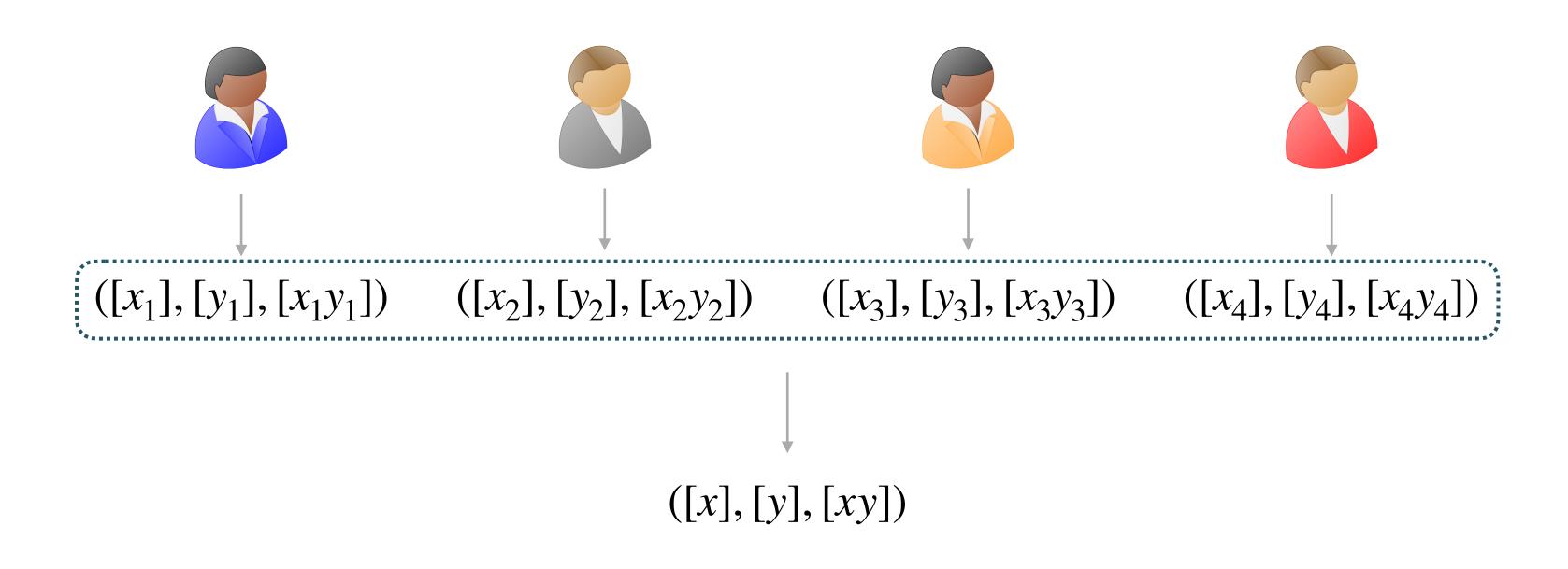


- Multiplication triple
- Triple known to party X





- Triple generation framework of [CP17] •
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Triple extraction protocol

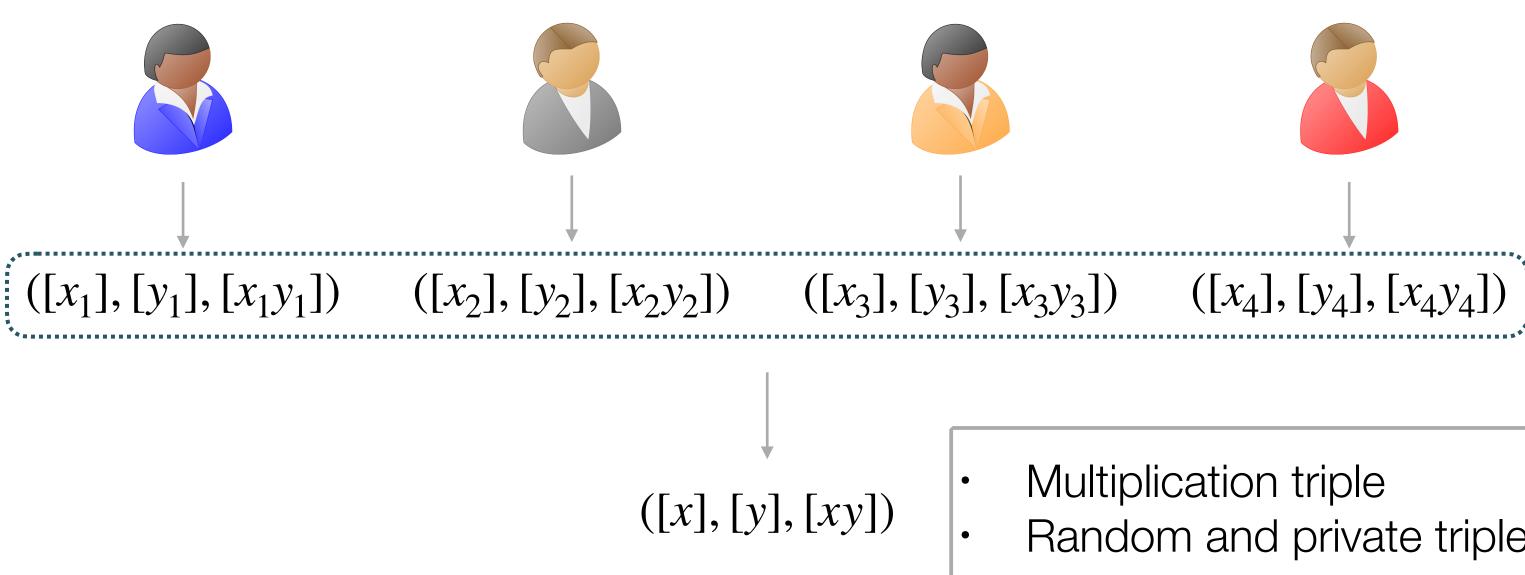
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Overview - Generating Multiplication Triples

- Triple generation framework of [CP17] •
 - Triple sharing protocol



Triple extraction protocol

Multiplication triple

Triple known to party X

Multiplication triple 🗸 Random and private triple 🗸



Perfect HMPC

- Open Problem [PR18]: Perfectly secure MPC protocol over hybrid network •
 - Two synchronous rounds •
 - Tolerating t < n/3 corruptions
 - With synchronous broadcast channel •
 - Guaranteed output delivery •
- Input provision impossible in this setting [PR18] •

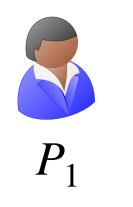
- Replicated Secret Sharing [ISN89]
 - $[s] = (s_1, s_2, s_3, s_4)$
 - $s = s_1 + s_2 + s_3 + s_4$

Replicated Secret Sharing [ISN89] •

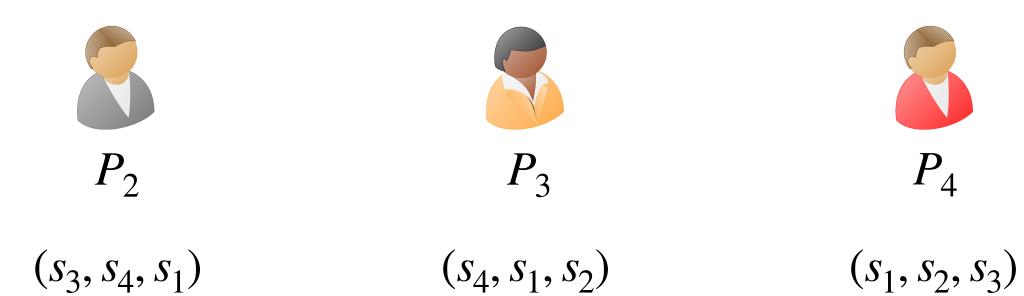
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•
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•
$$P_i$$
 does not have s_i

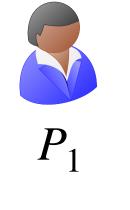


 (s_2, s_3, s_4)



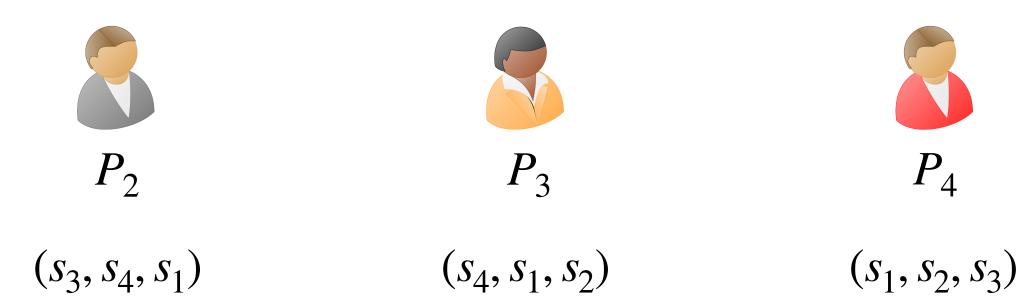


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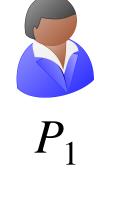
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- P_i does not have s_i
 - All other parties except P_i have S_i



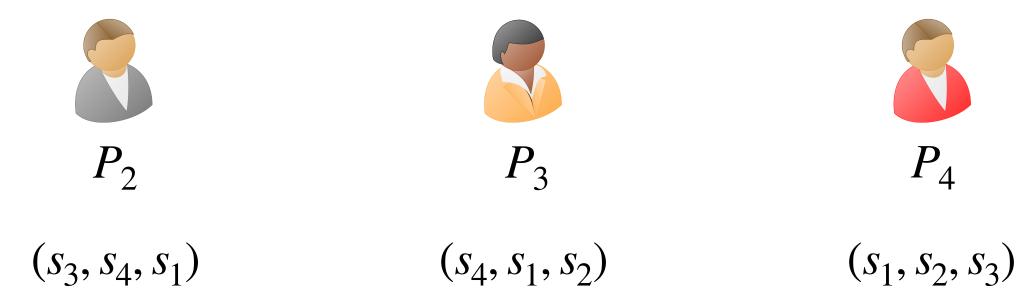


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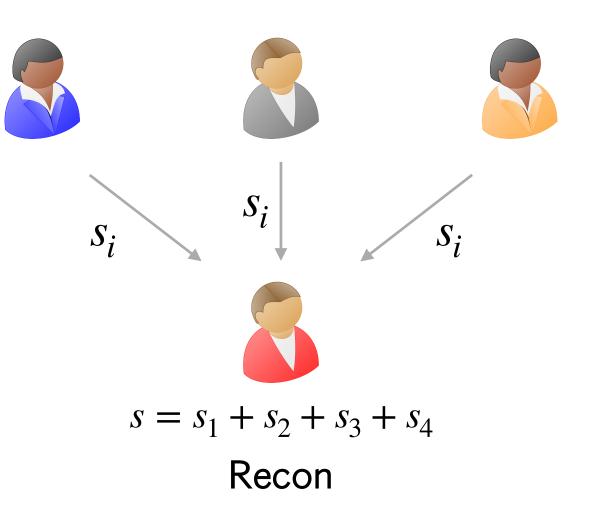


$$[cs] = (cs_1, cs_2, cs_3, cs_4)$$

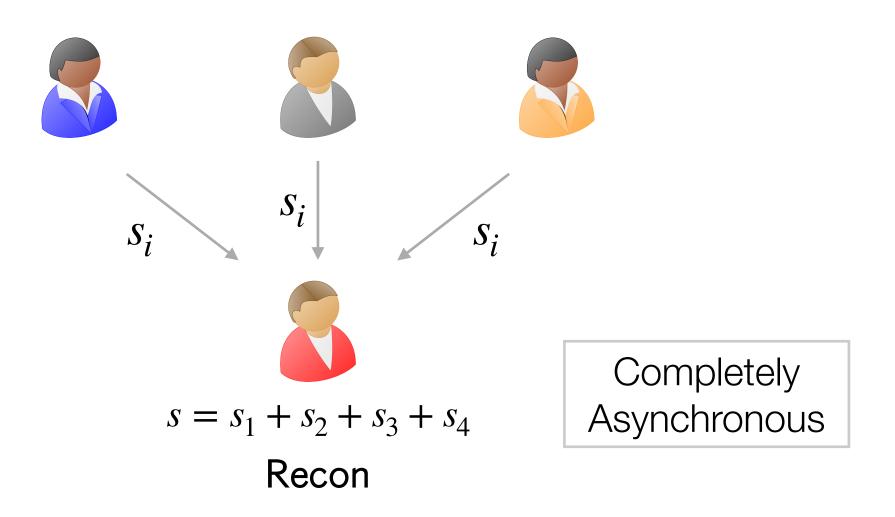
$$[s+s'] = (s_1 + s'_1, s_2 + s'_2, s_3 + s'_3, s_4 + s'_4)$$



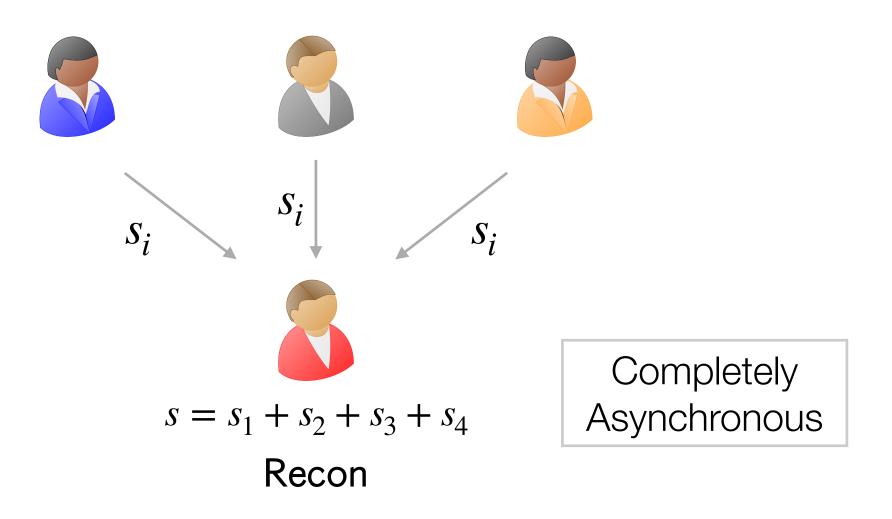
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 - P_j sends s_i to P_i
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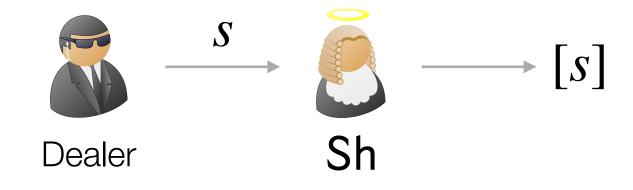


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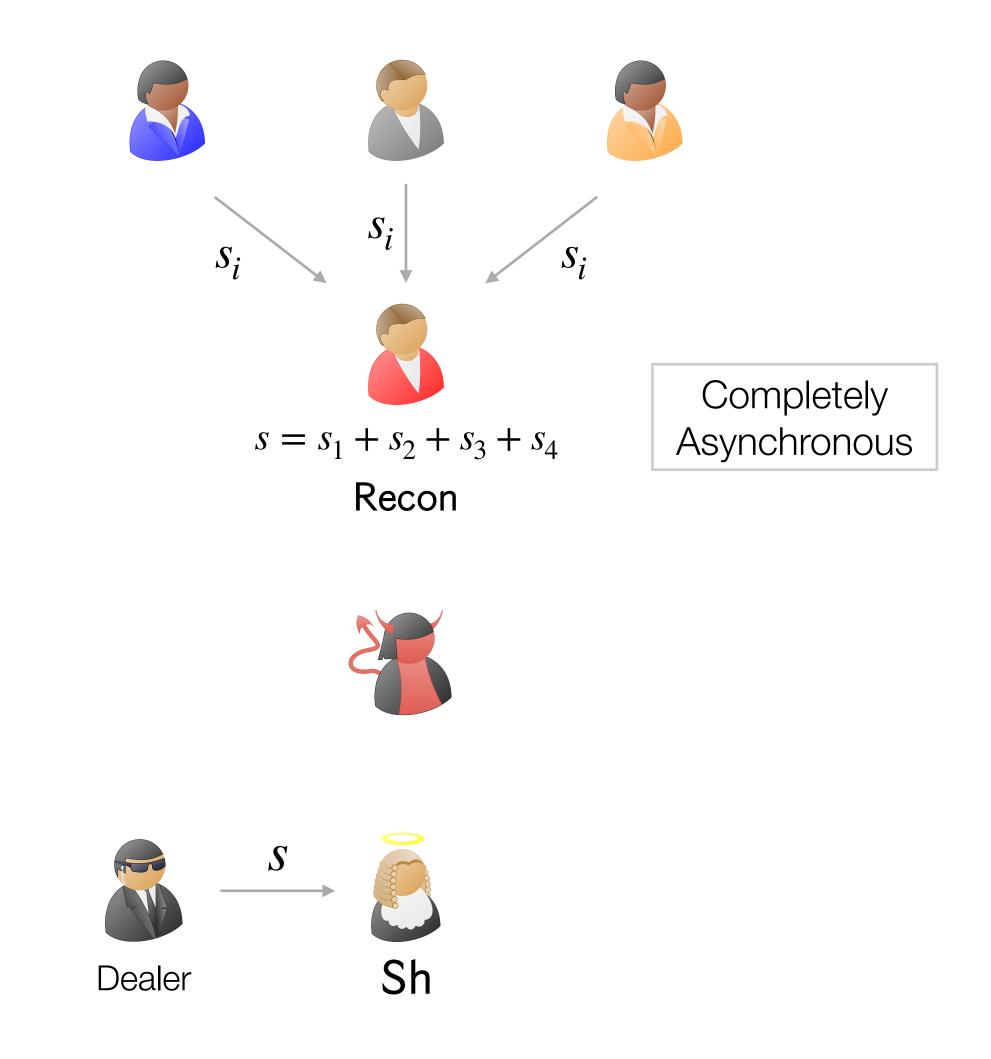


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- VSS with Party Elimination
 - Secret sharing or dispute set

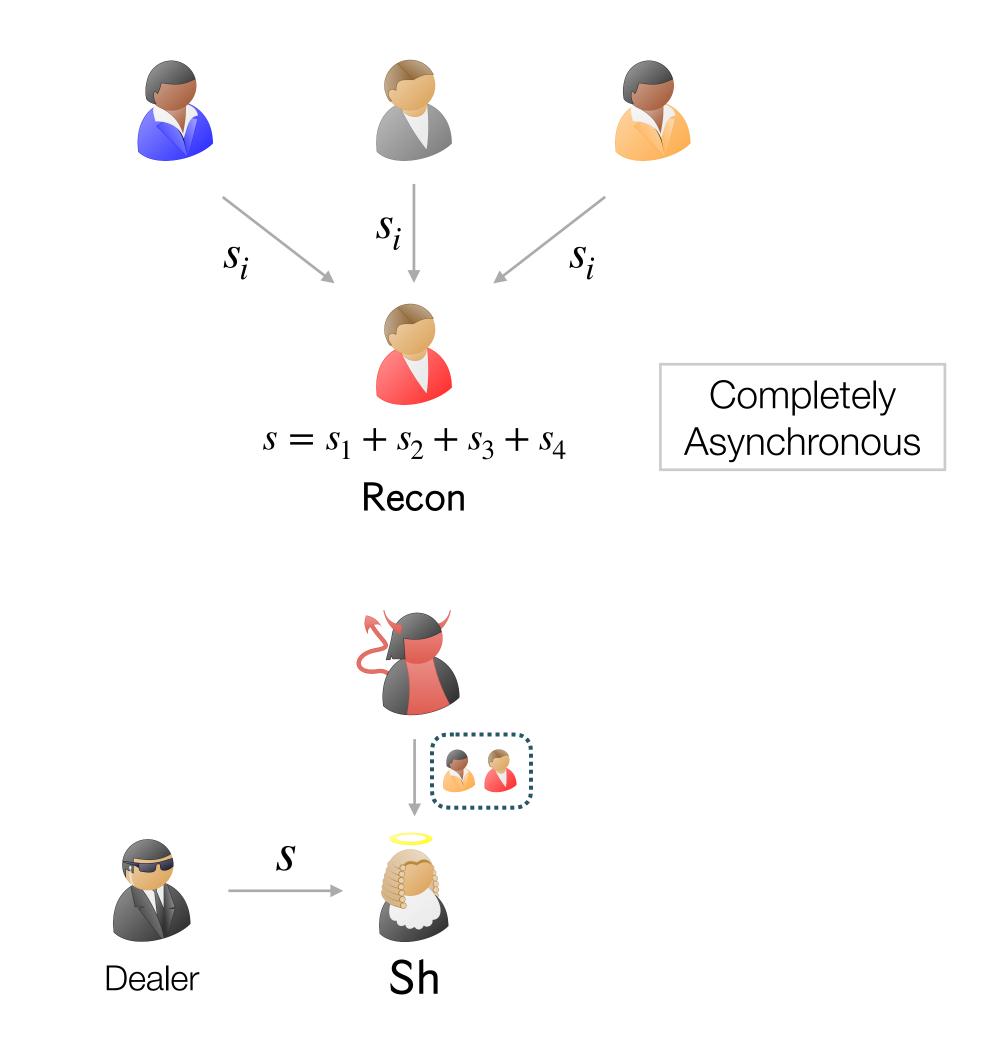




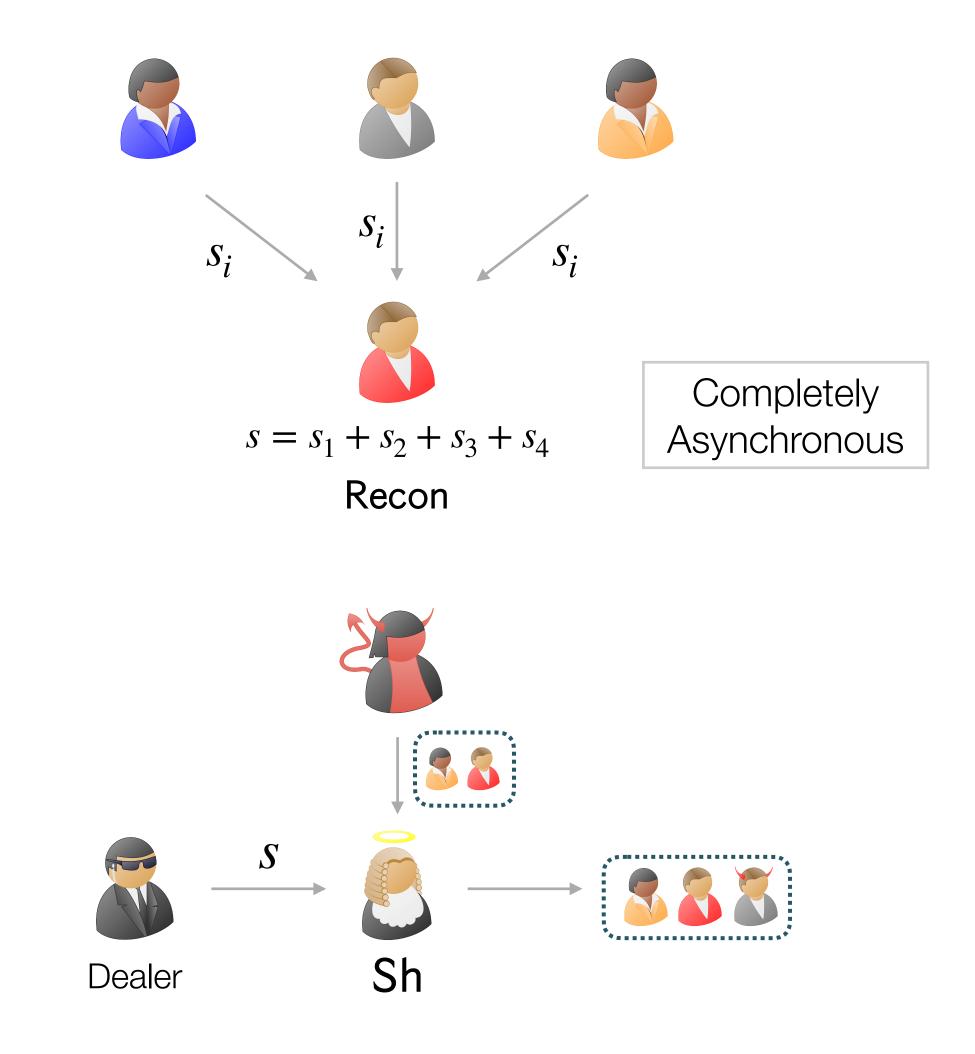
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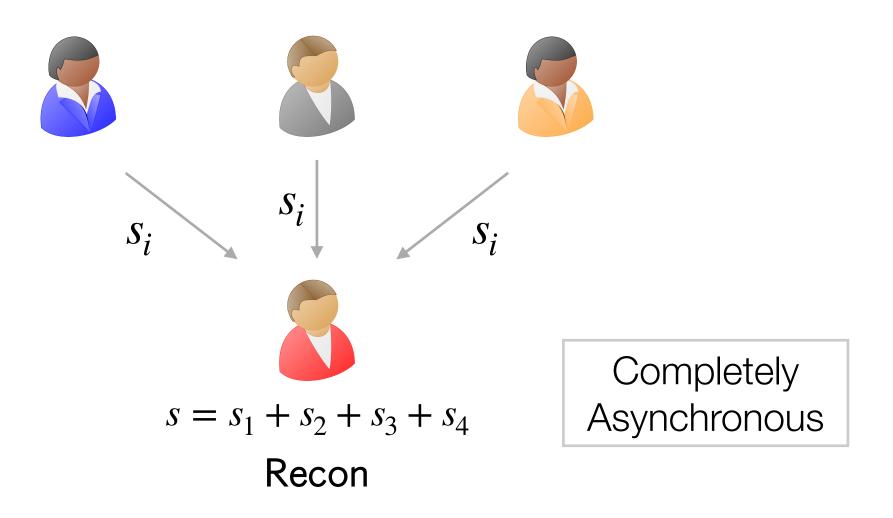
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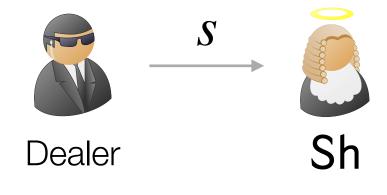


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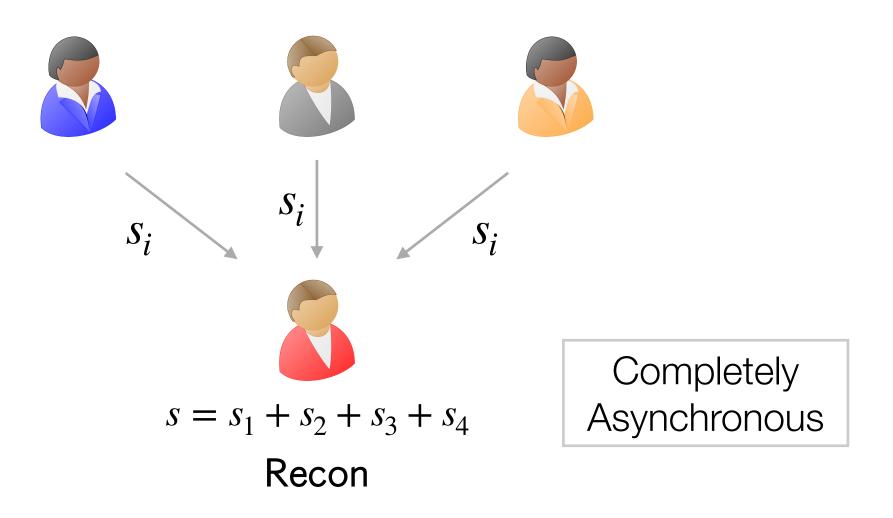


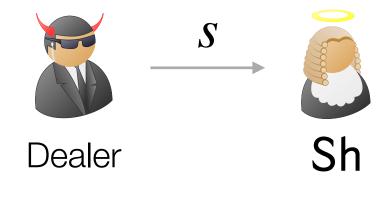
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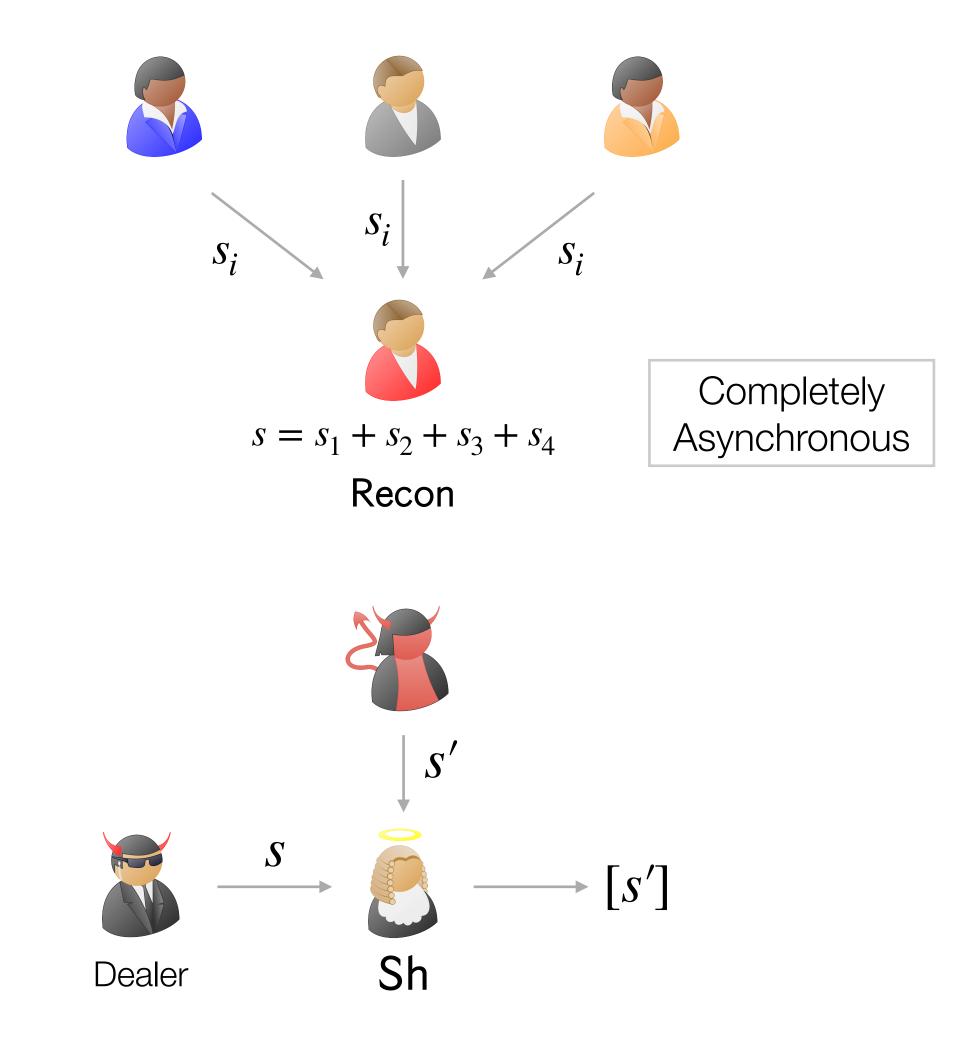


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- Round 1
 - D sends share to each party
 - Parties exchange random pad for each common element in share

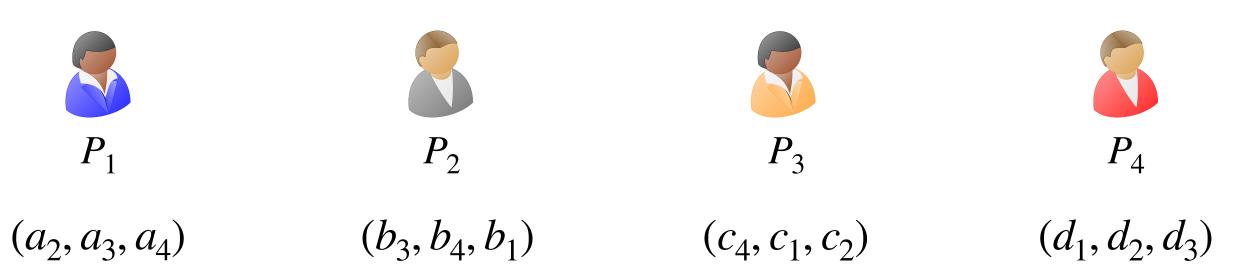




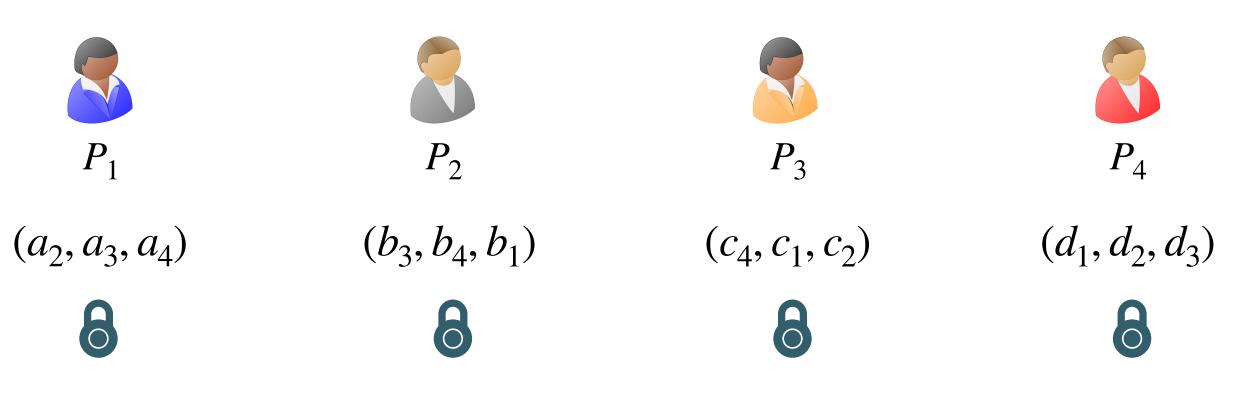




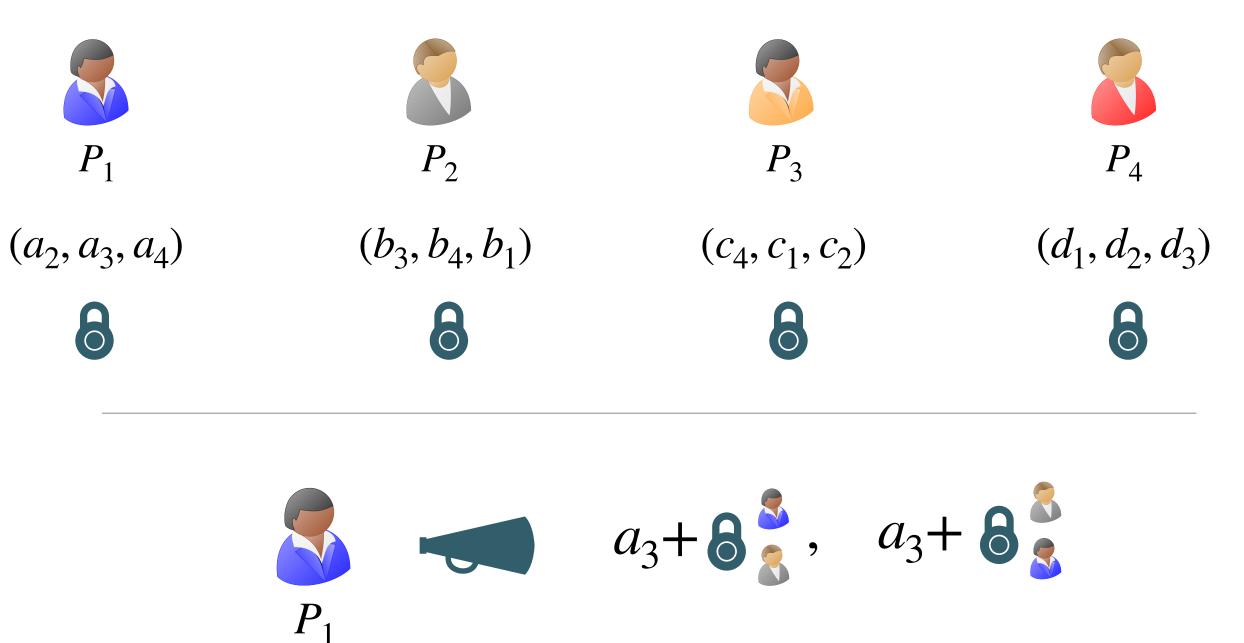
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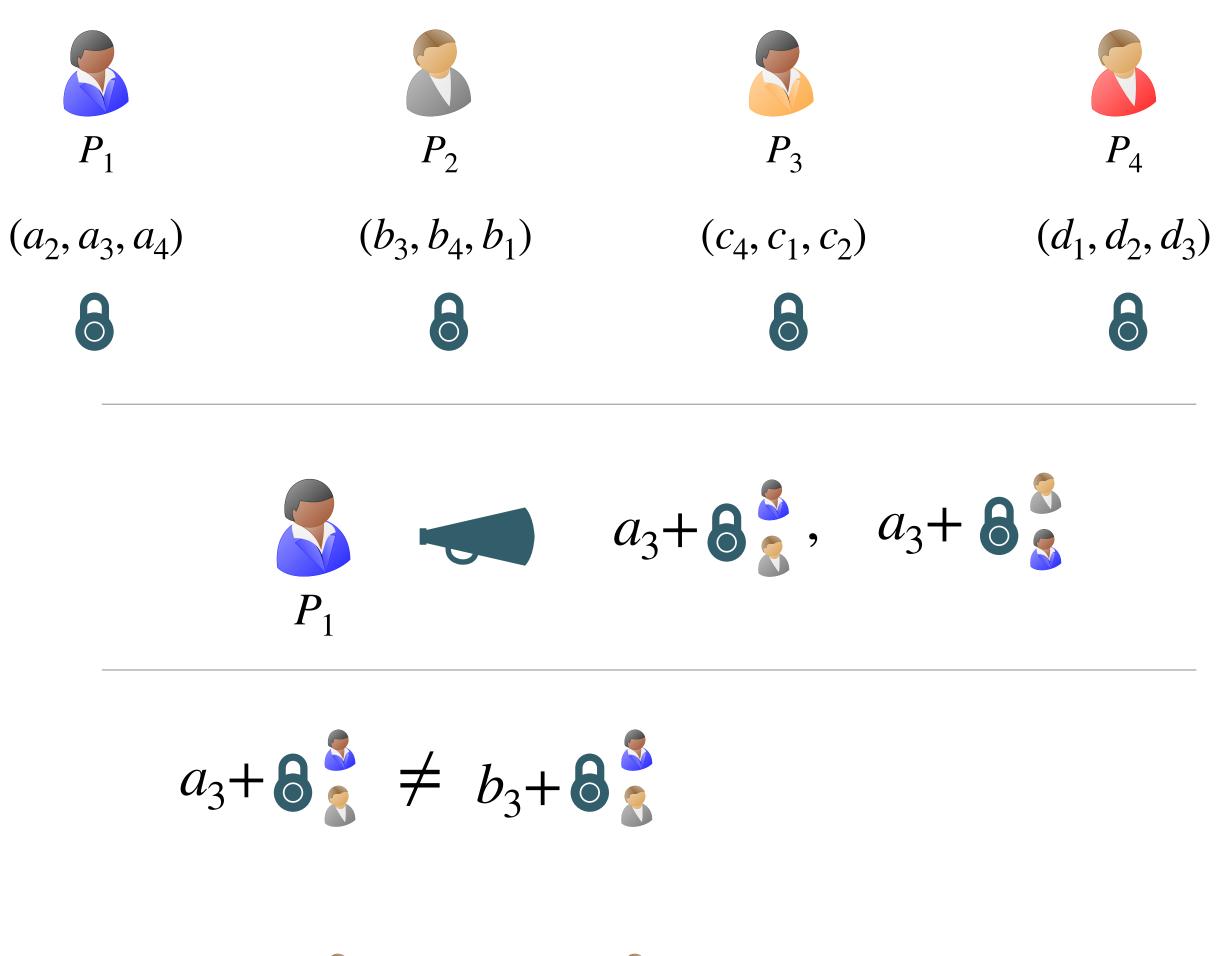
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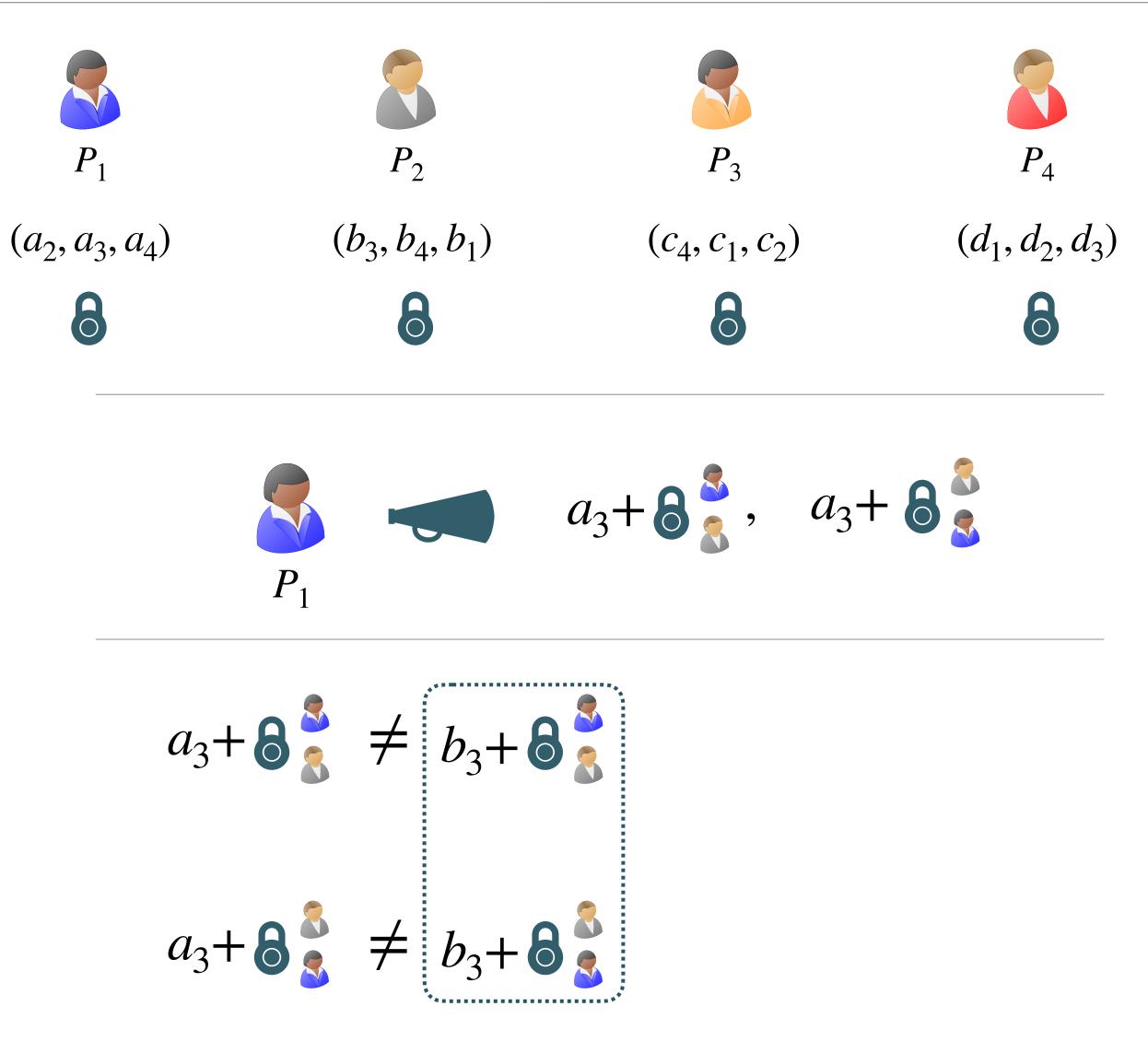


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- Local computation
 - If shares inconsistent, output dispute set
 - Else output with secret shares

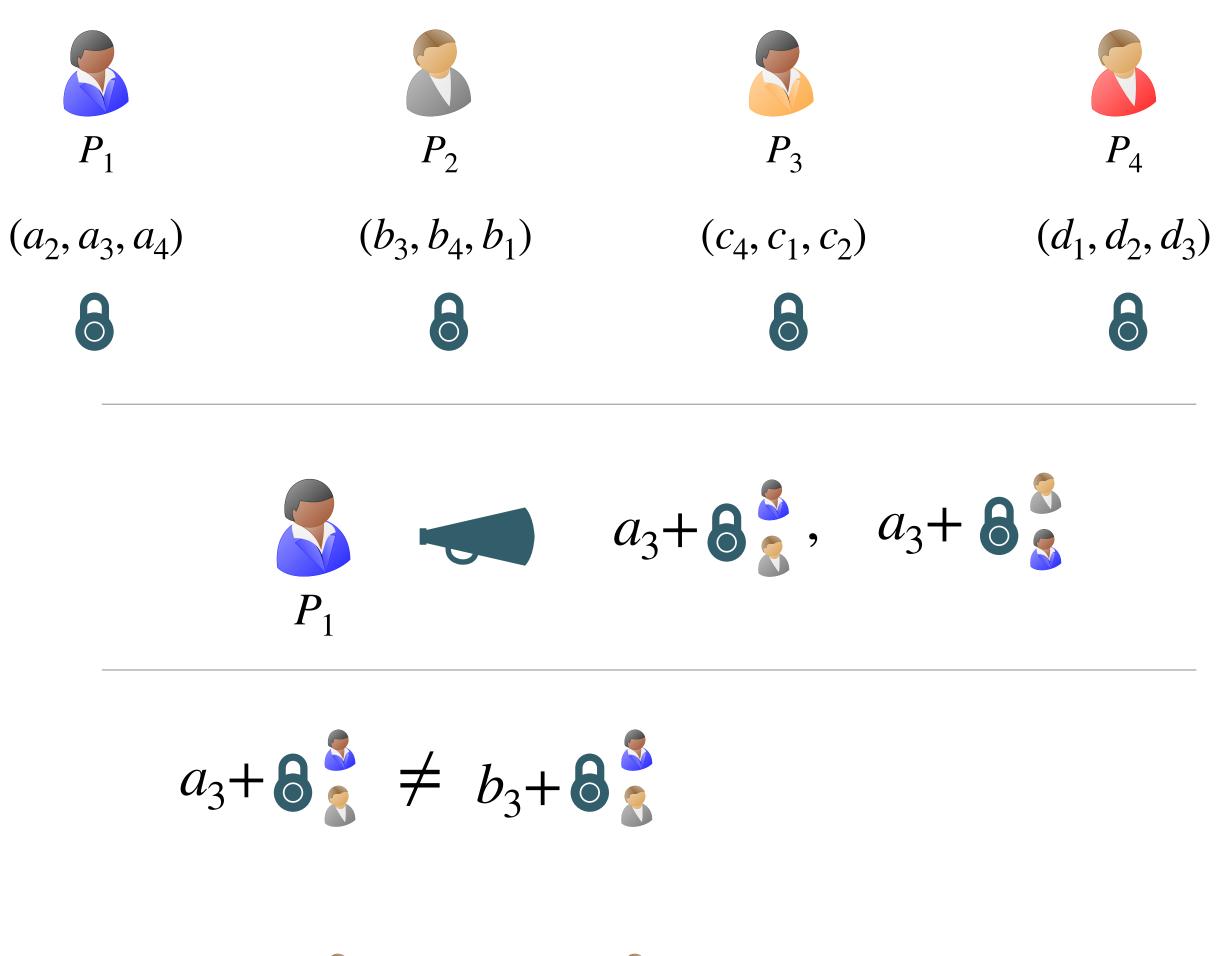


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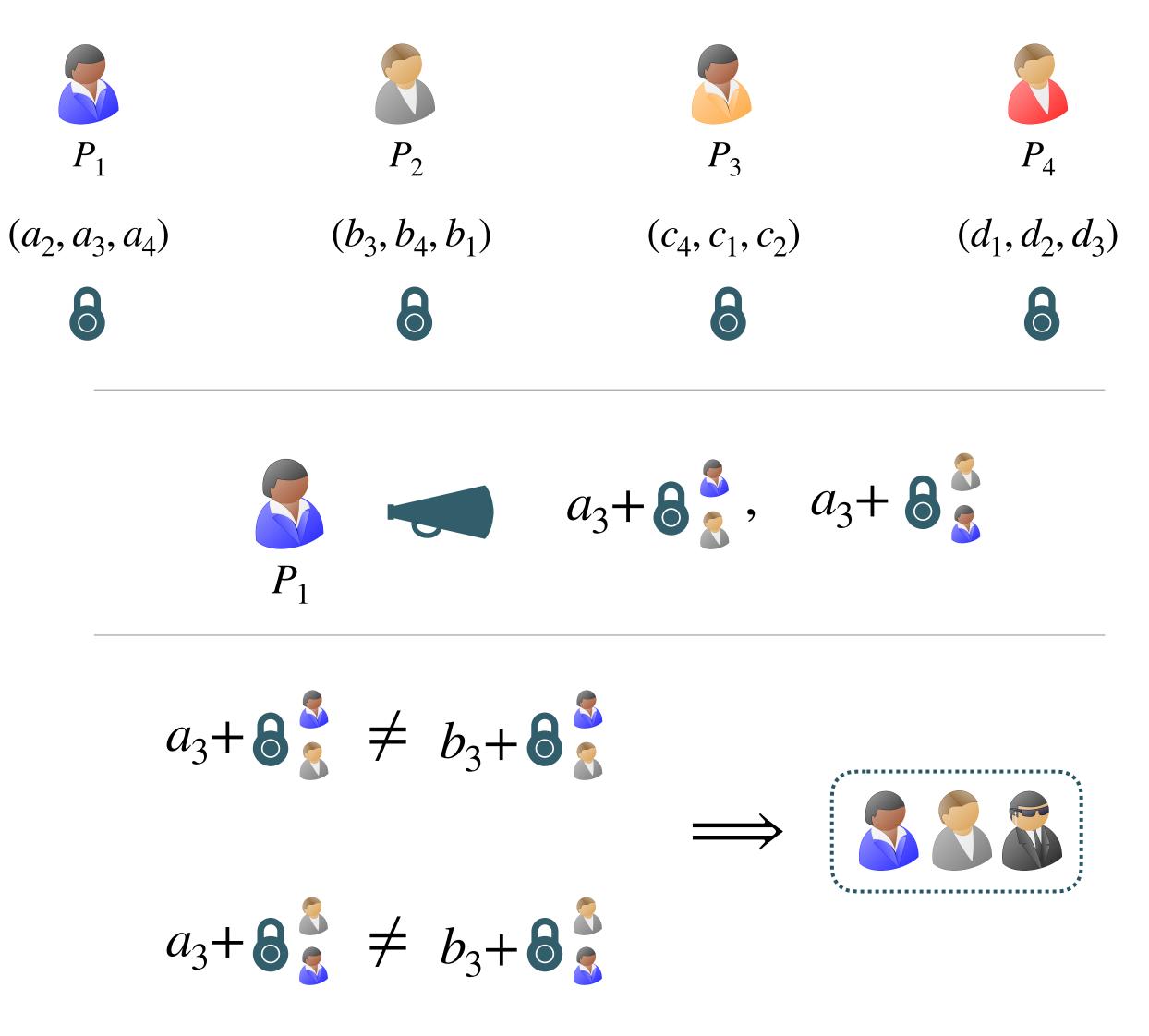


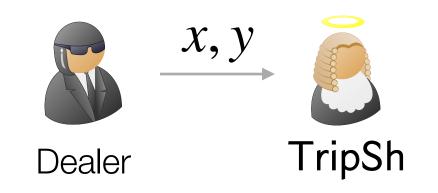
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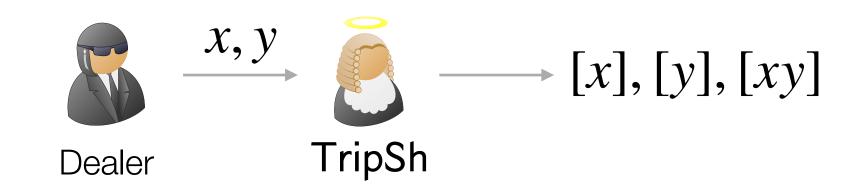
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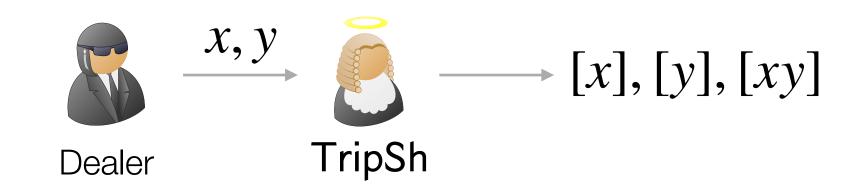




- Triple sharing with Party Elimination •
 - Verified multiplication triple or dispute set

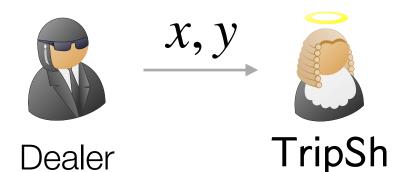


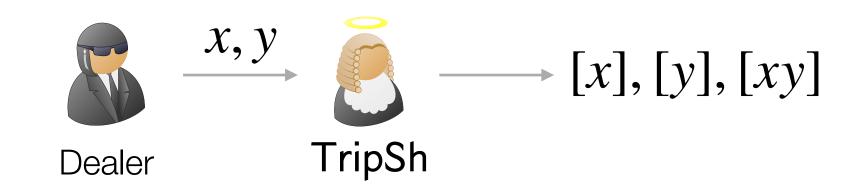
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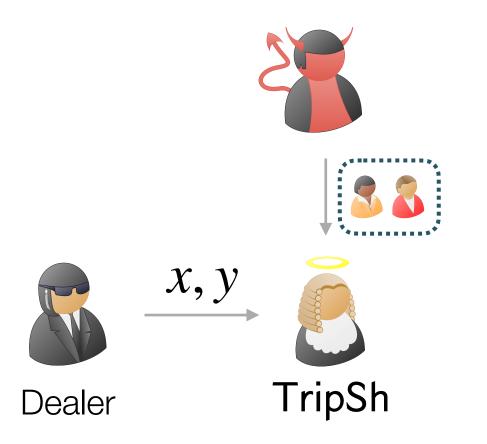
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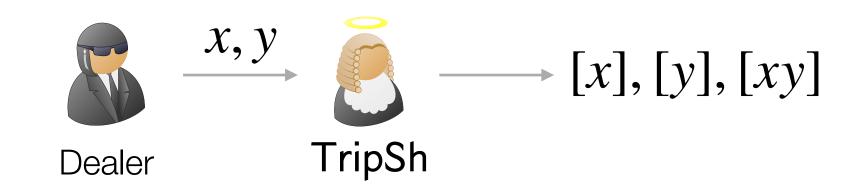




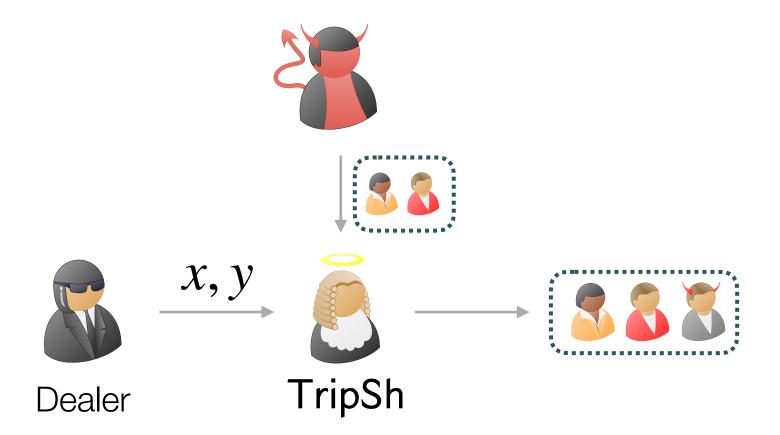


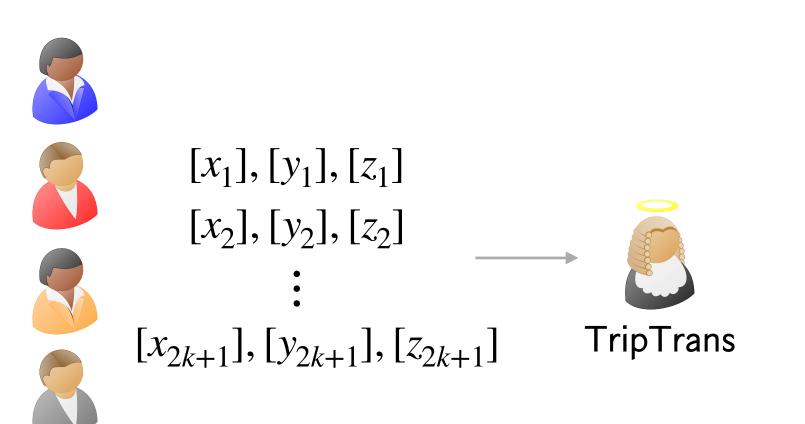
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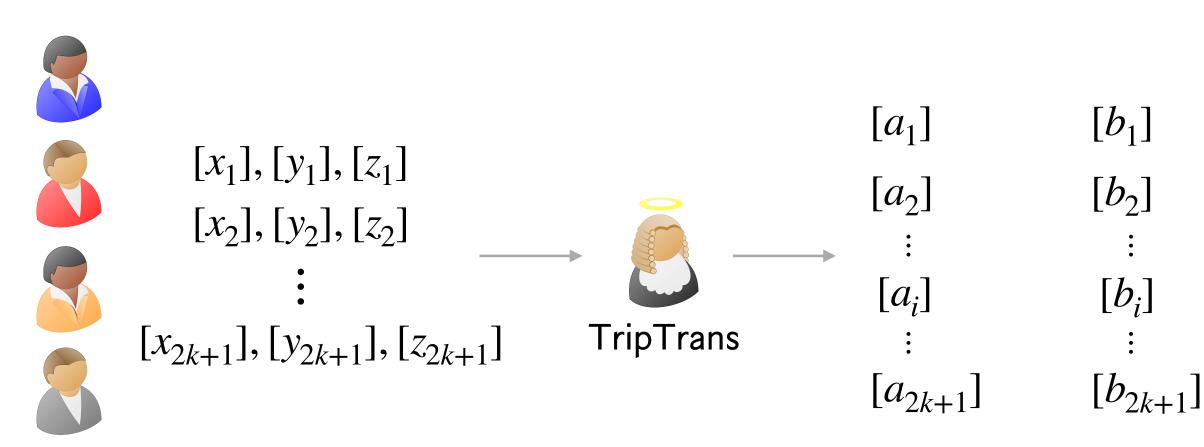


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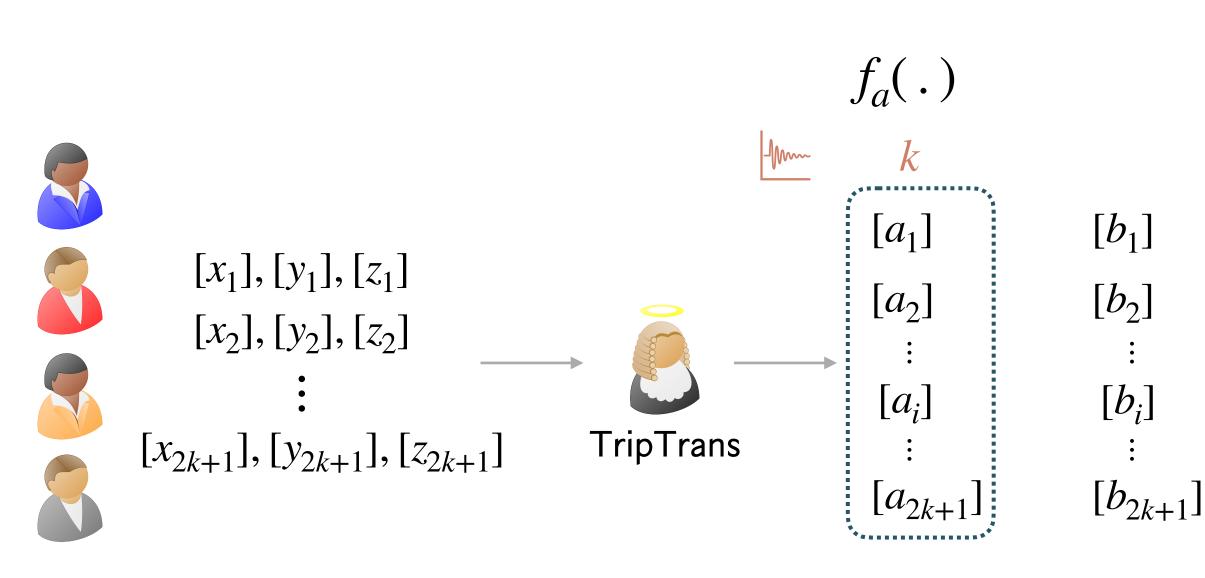


• Random triples \rightarrow correlated random triples



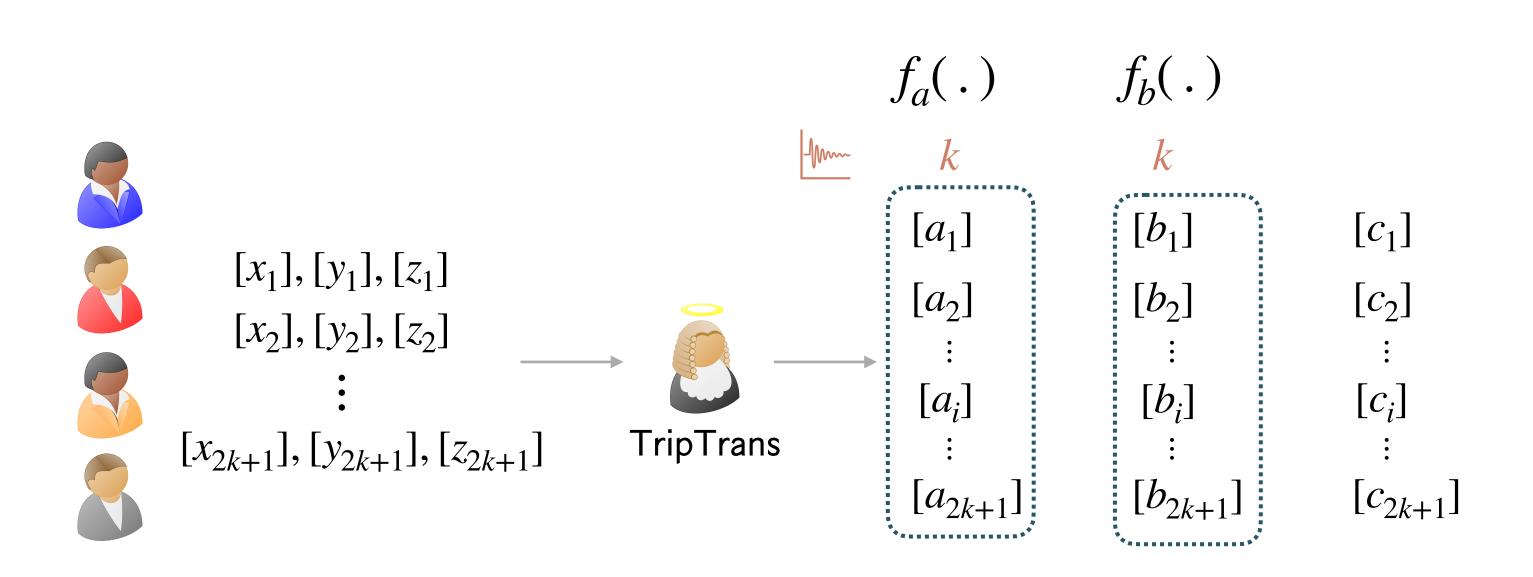
• Random triples \rightarrow correlated random triples

 $[c_1]$ $[c_2]$ $[C_i]$ $[c_{2k+1}]$

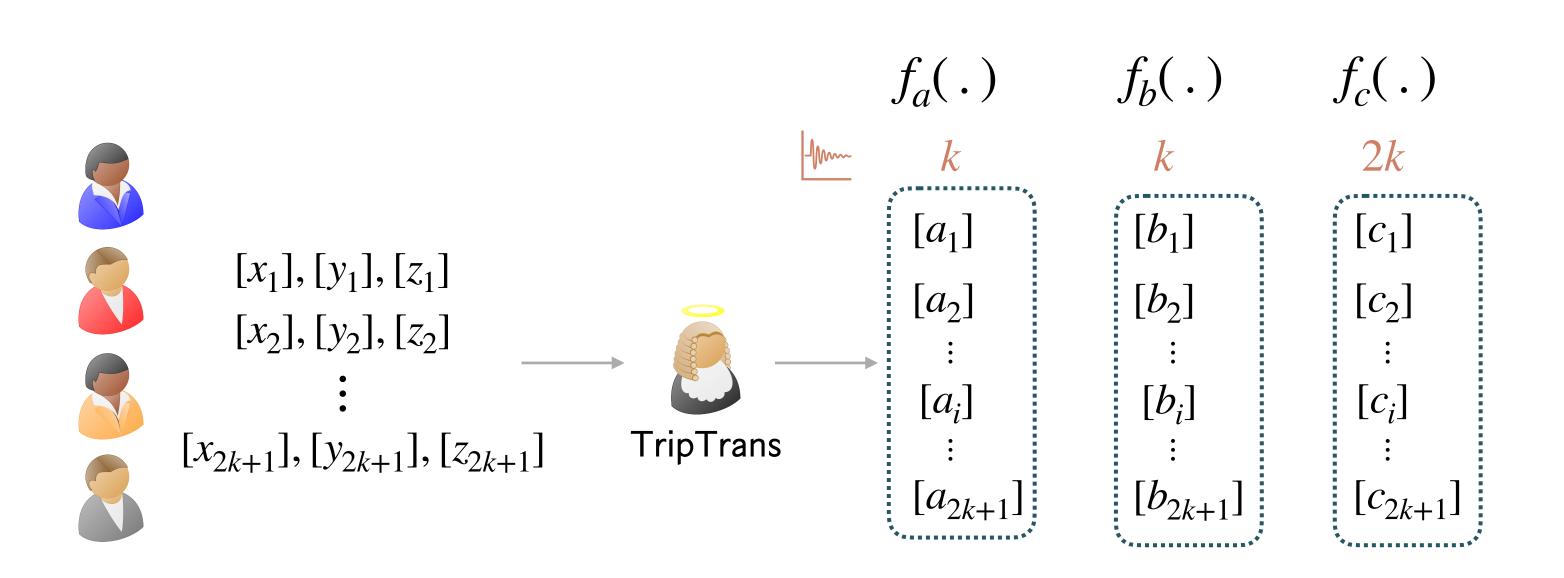


• Random triples \rightarrow correlated random triples

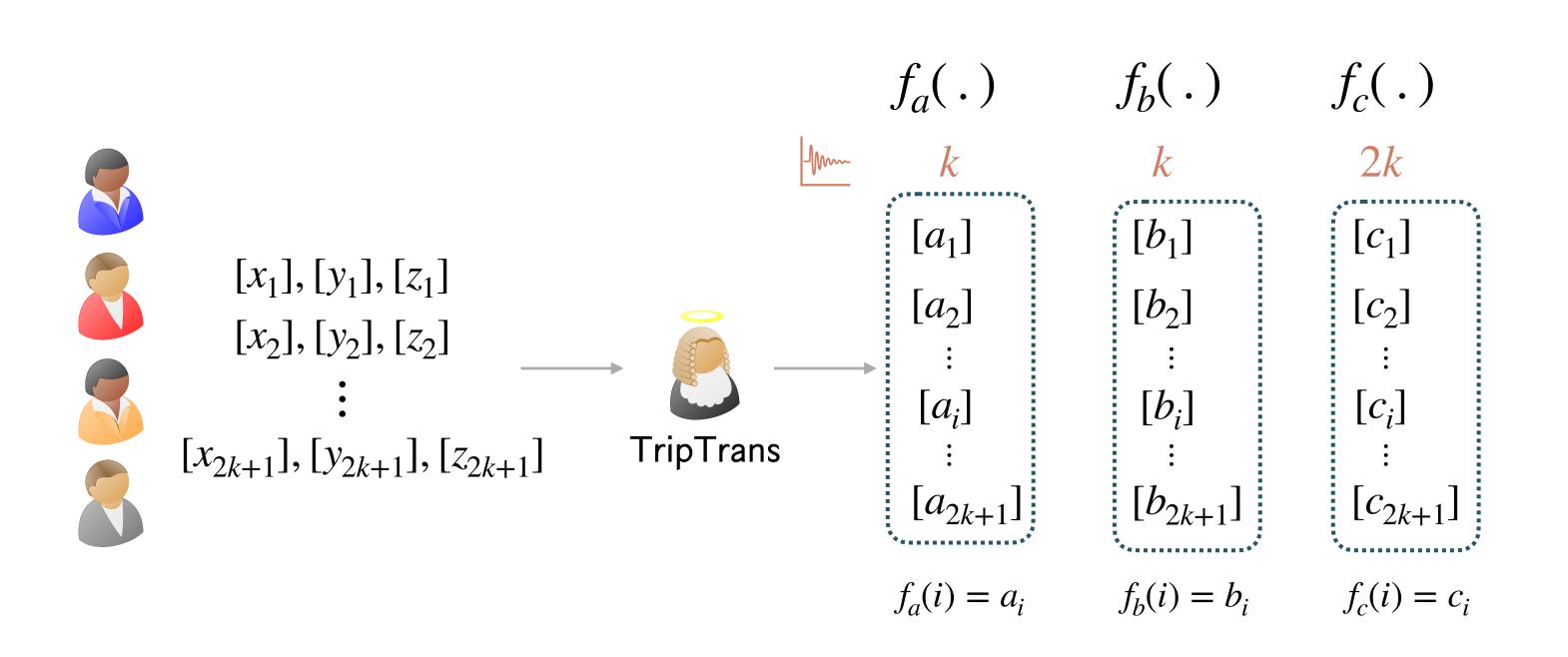
 $[c_{1}]$ $[c_{2}]$ \vdots $[c_{i}]$ \vdots $[c_{2k+1}]$



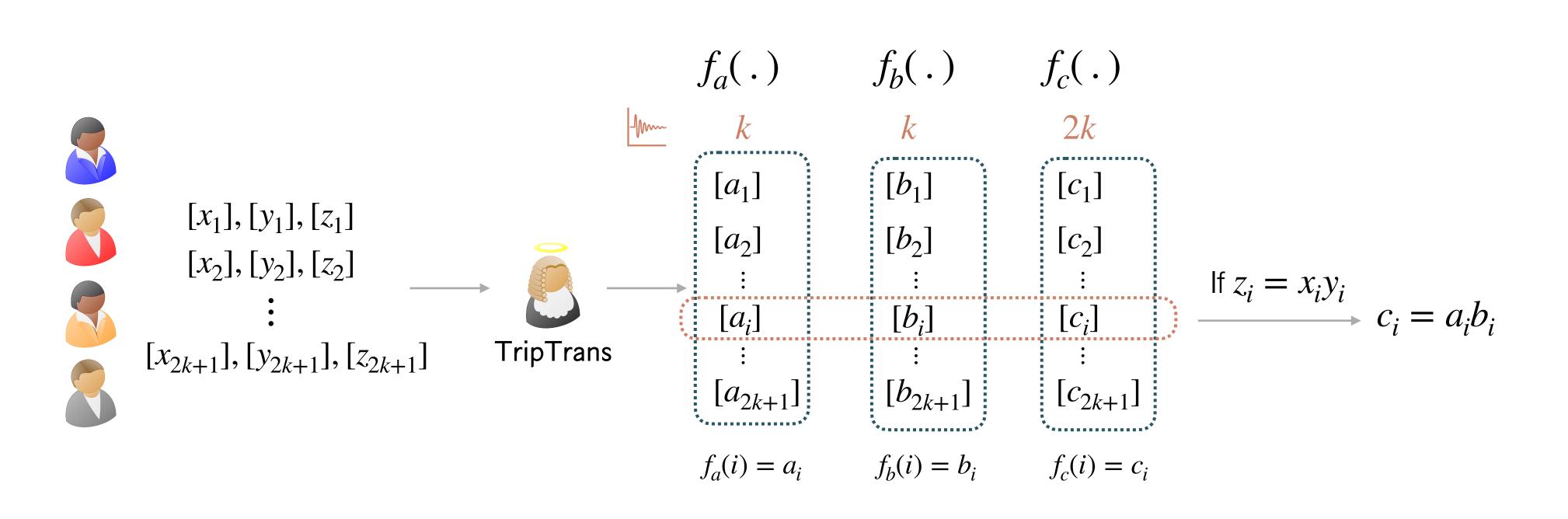
• Random triples \rightarrow correlated random triples



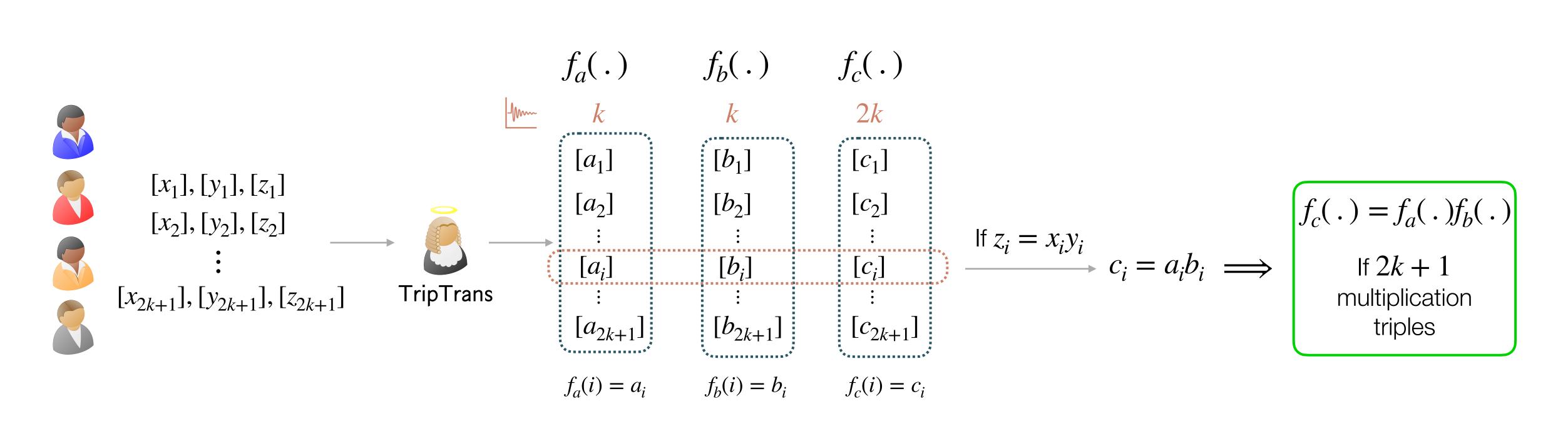
Random triples \rightarrow correlated random triples •



Random triples \rightarrow correlated random triples •

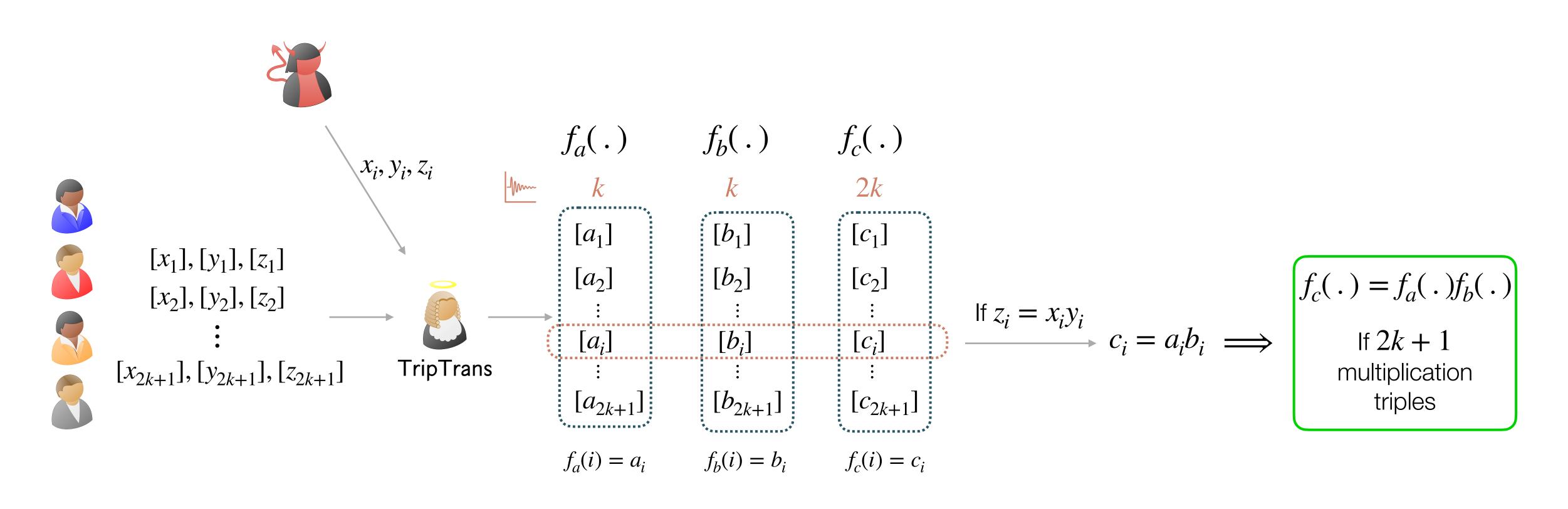


• Random triples \rightarrow correlated random triples



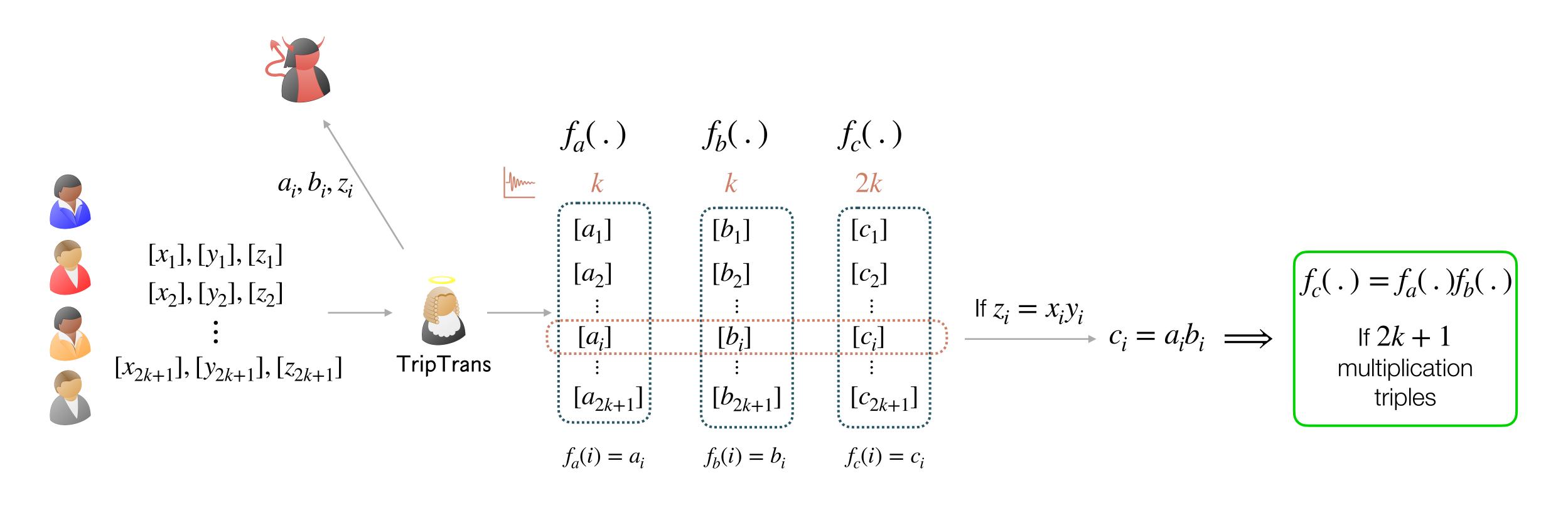
• Random triples \rightarrow correlated random triples

Perfect HMPC - Triple Transform Functionality



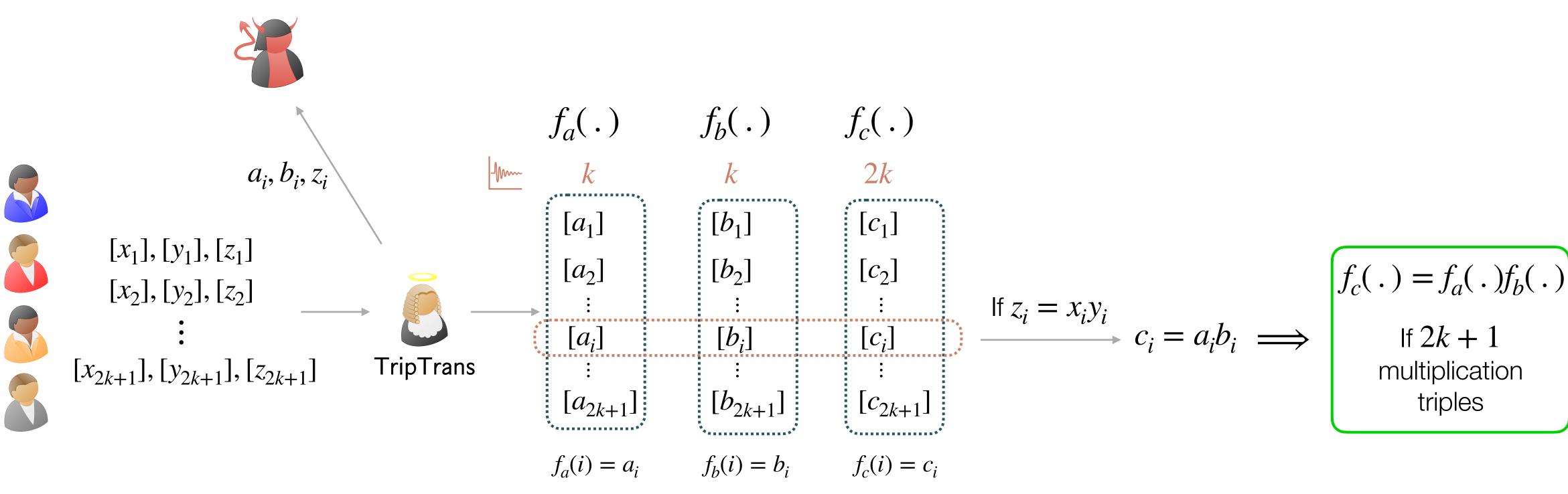
• Random triples \rightarrow correlated random triples

Perfect HMPC - Triple Transform Functionality



• Random triples \rightarrow correlated random triples

Perfect HMPC - Triple Transform Functionality



- Random triples \rightarrow correlated random triples
- Completely asynchronous instantiation in [CP17] •

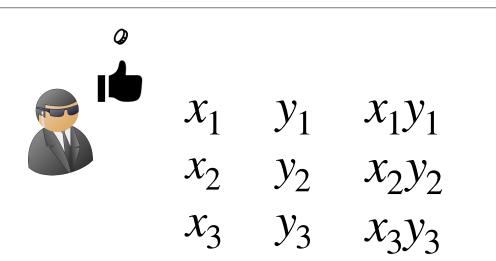








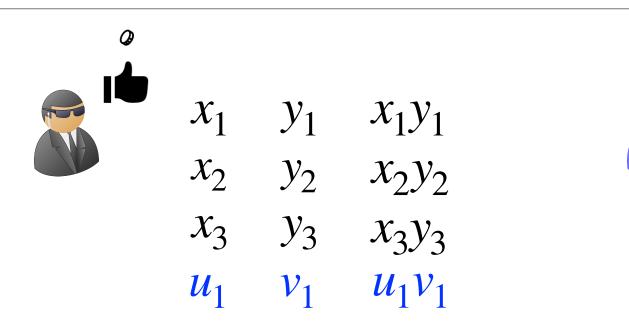


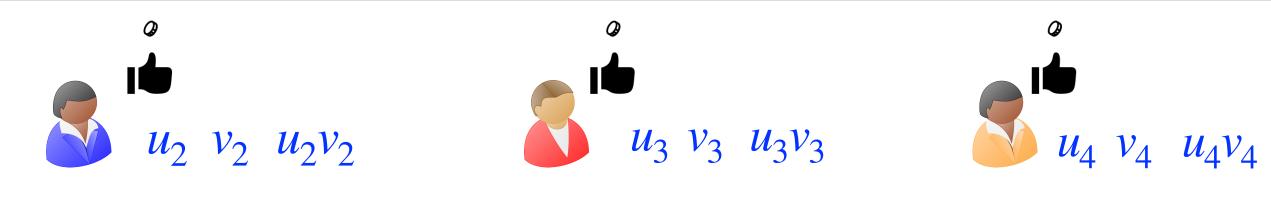


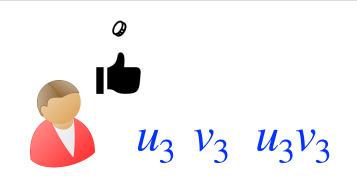


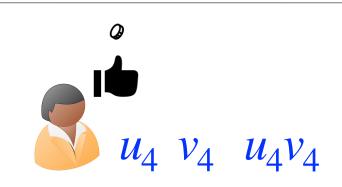


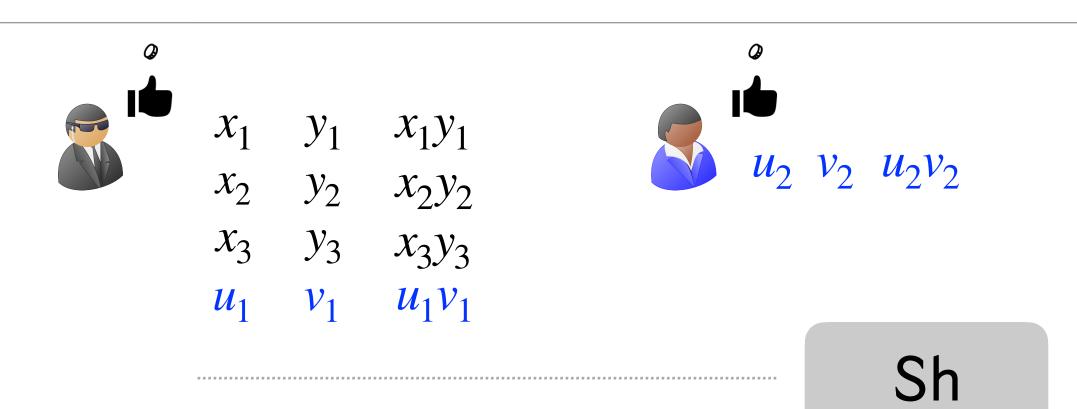




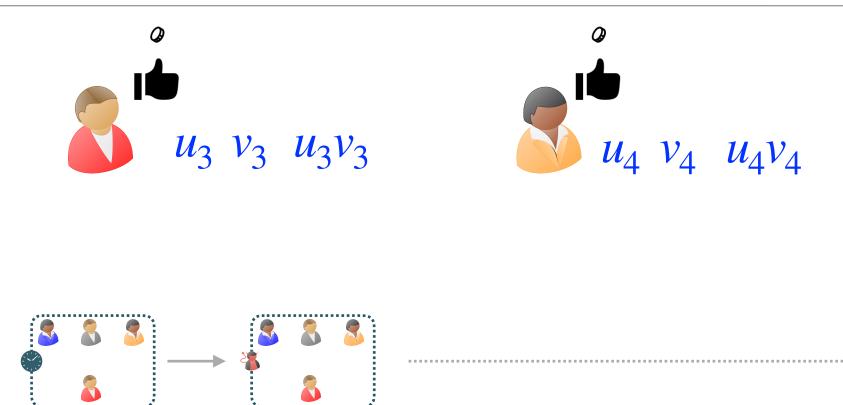




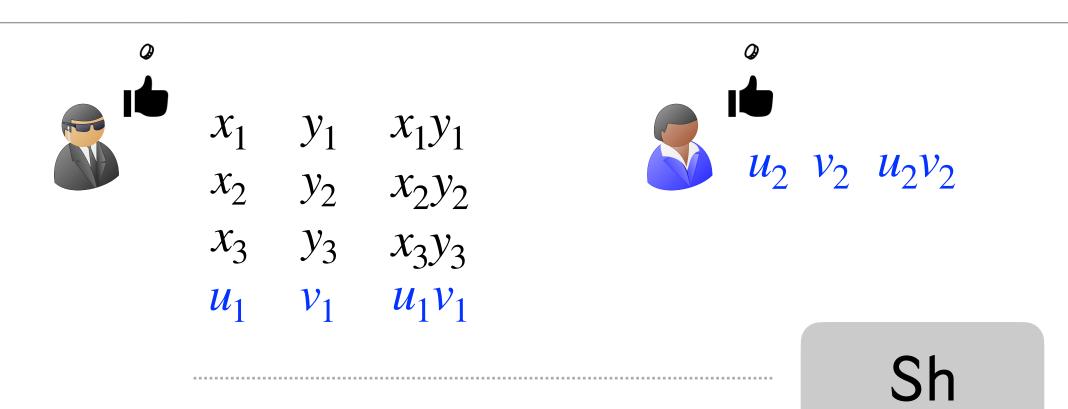




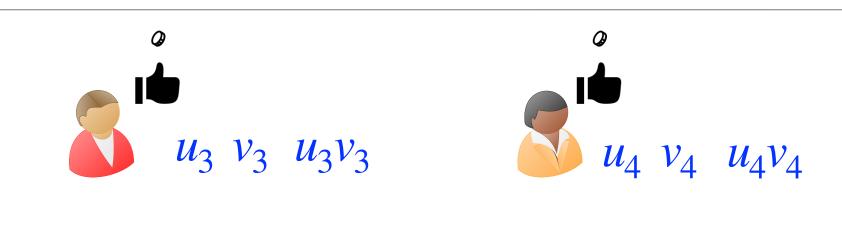
 $\begin{bmatrix} x_1 \\ y_1 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \end{bmatrix}$ $\begin{bmatrix} x_2 \\ z_2 \end{bmatrix} \begin{bmatrix} y_2 \\ z_2 \end{bmatrix}$ $\begin{bmatrix} x_3 \\ z_3 \end{bmatrix} \begin{bmatrix} y_3 \\ z_3 \end{bmatrix}$

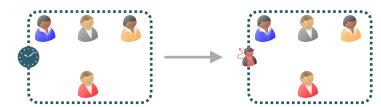


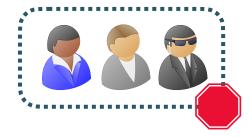
 $\begin{bmatrix} u_1 \\ v_1 \end{bmatrix} \begin{bmatrix} v_1 \\ w_1 \end{bmatrix}$ $\begin{bmatrix} u_2 \\ v_2 \end{bmatrix} \begin{bmatrix} v_2 \\ w_2 \end{bmatrix}$ $\begin{bmatrix} u_3 \\ v_3 \end{bmatrix} \begin{bmatrix} v_3 \\ w_3 \end{bmatrix}$ $\begin{bmatrix} u_4 \end{bmatrix} \begin{bmatrix} v_4 \end{bmatrix} \begin{bmatrix} v_4 \end{bmatrix}$



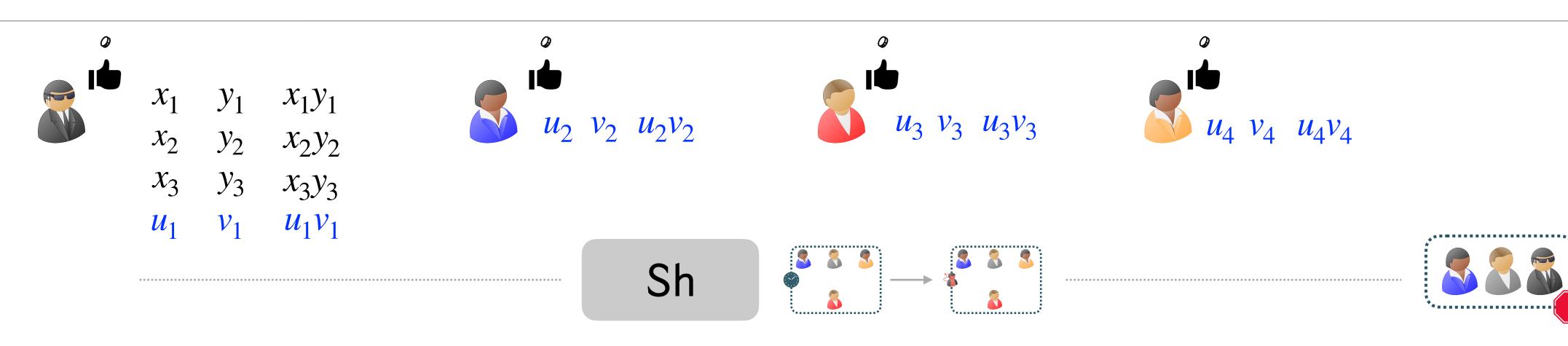
 $\begin{bmatrix} x_1 \\ y_1 \end{bmatrix} \begin{bmatrix} z_1 \\ z_2 \end{bmatrix}$ $\begin{bmatrix} x_2 \\ z_2 \end{bmatrix} \begin{bmatrix} y_2 \\ z_2 \end{bmatrix}$ $\begin{bmatrix} x_3 \\ z_3 \end{bmatrix} \begin{bmatrix} y_3 \\ z_3 \end{bmatrix}$

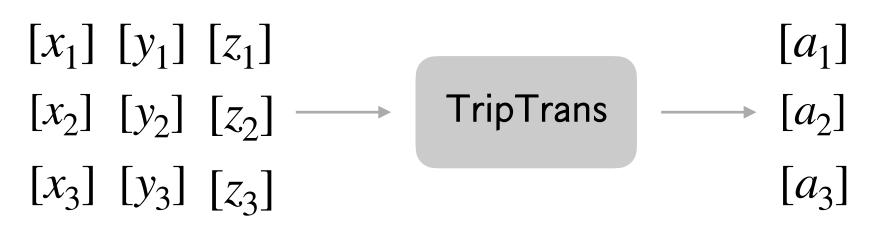






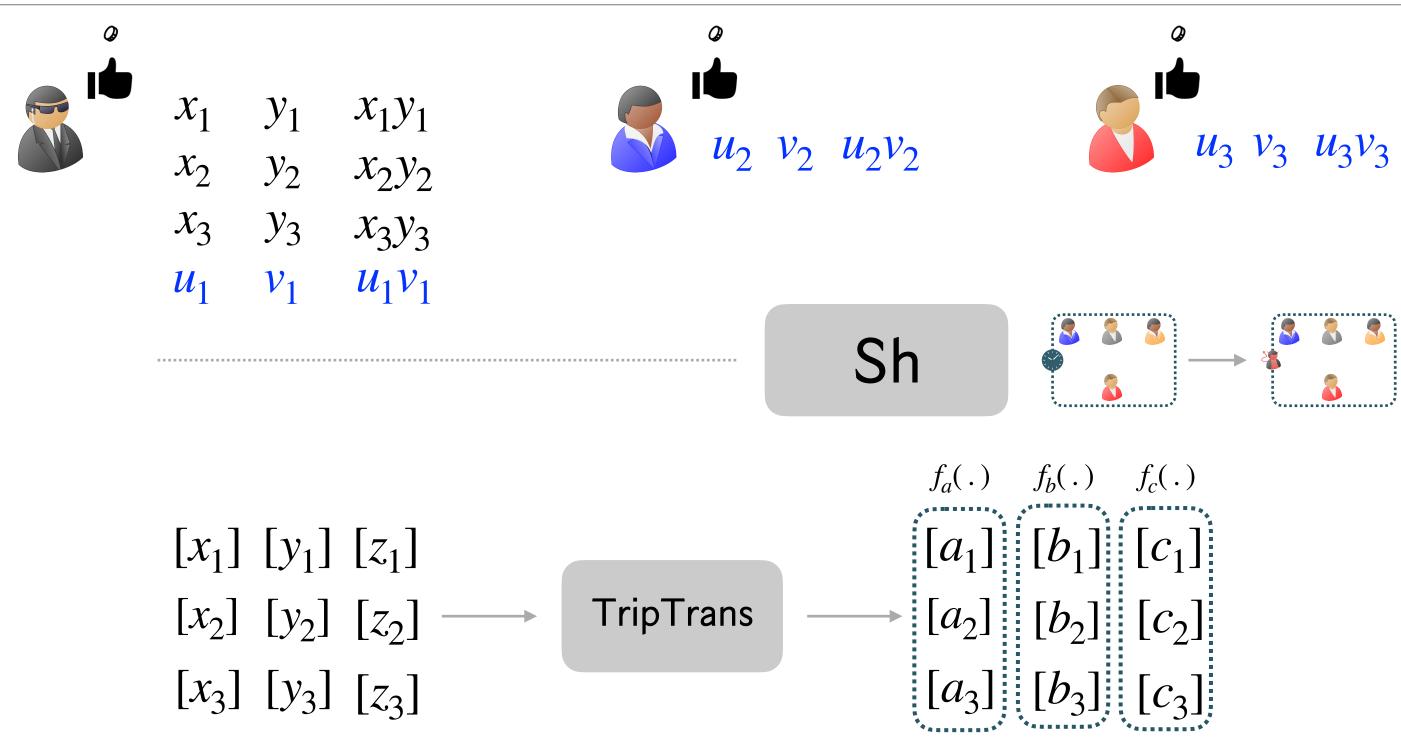
 $\begin{bmatrix} u_1 \\ v_1 \end{bmatrix} \begin{bmatrix} v_1 \\ w_1 \end{bmatrix}$ $\begin{bmatrix} u_2 \\ v_2 \end{bmatrix} \begin{bmatrix} v_2 \\ w_2 \end{bmatrix}$ $\begin{bmatrix} u_3 \\ v_3 \end{bmatrix} \begin{bmatrix} v_3 \\ w_3 \end{bmatrix}$ $\begin{bmatrix} u_4 \end{bmatrix} \begin{bmatrix} v_4 \end{bmatrix} \begin{bmatrix} v_4 \end{bmatrix}$

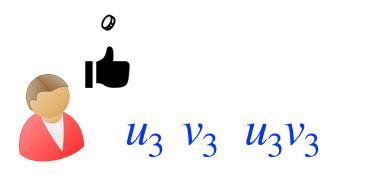


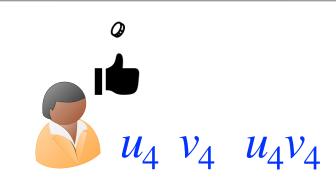


 $[a_1] [b_1] [c_1]$ $[a_2] [b_2] [c_2]$

 $[u_1] [v_1] [w_1]$ $[u_2] [v_2] [w_2]$ $[a_3] [b_3] [c_3] [u_3] [v_3] [w_3]$ $[u_4] [v_4] [w_4]$

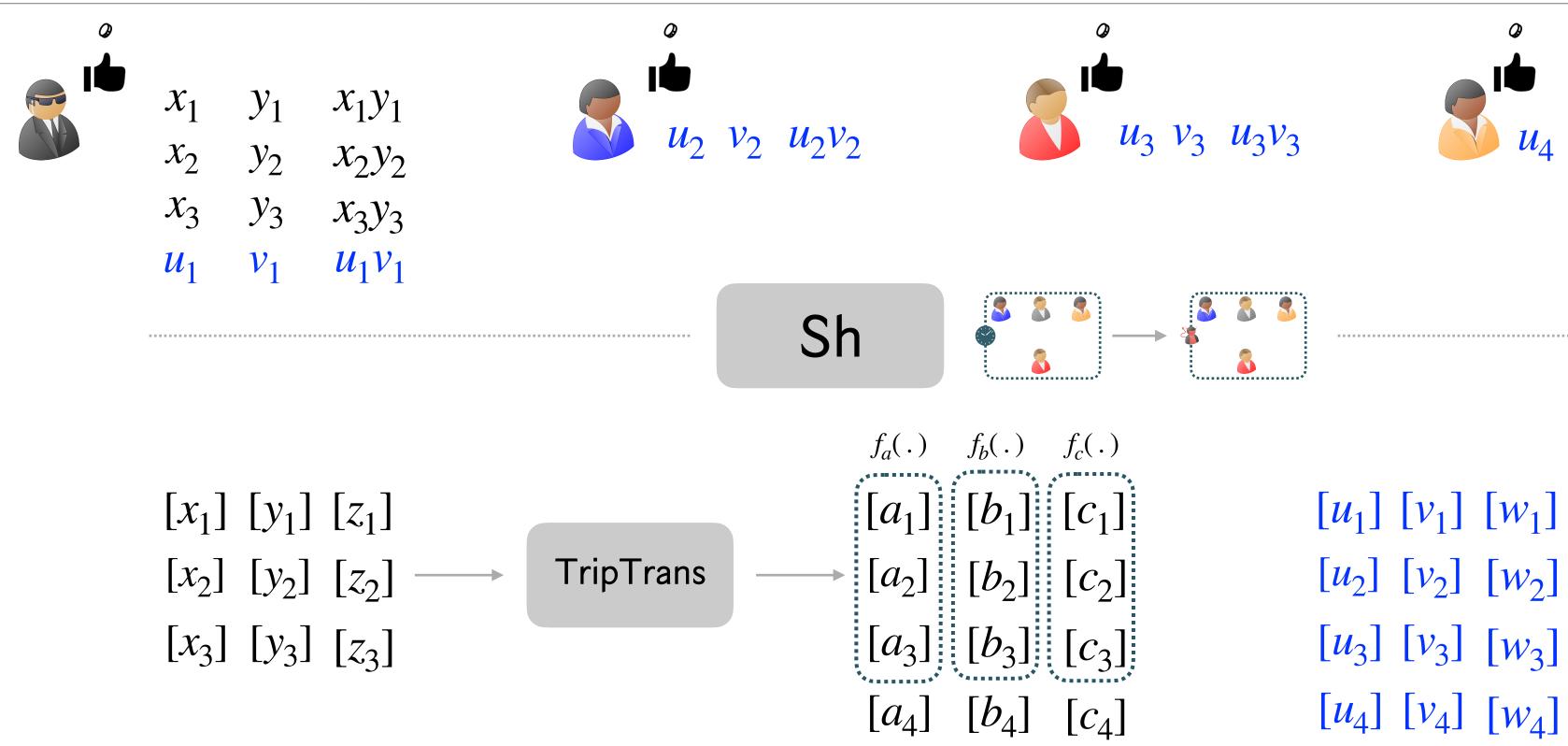


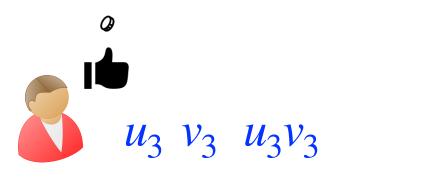






 $[u_1] [v_1] [w_1]$ $[u_2] [v_2] [w_2]$ $[u_3] [v_3] [w_3]$ $[u_4] [v_4] [w_4]$

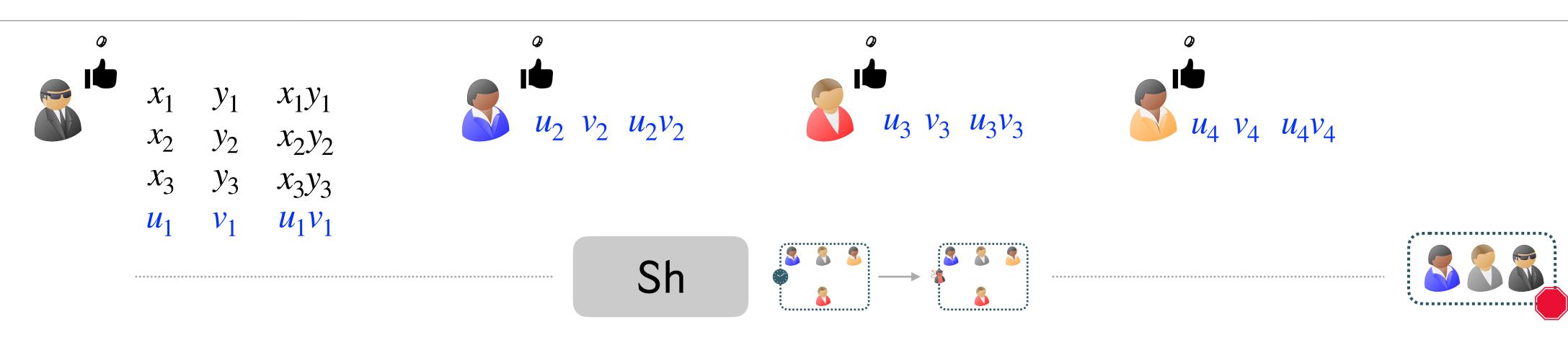


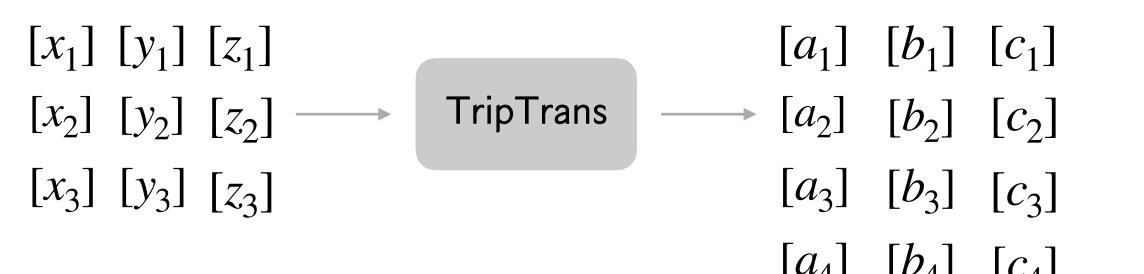


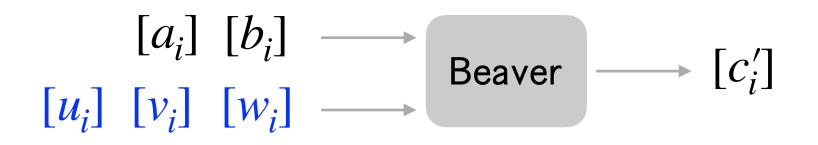




 $[u_1] [v_1] [w_1]$ $[u_2] [v_2] [w_2]$ $[u_4] [v_4] [w_4]$

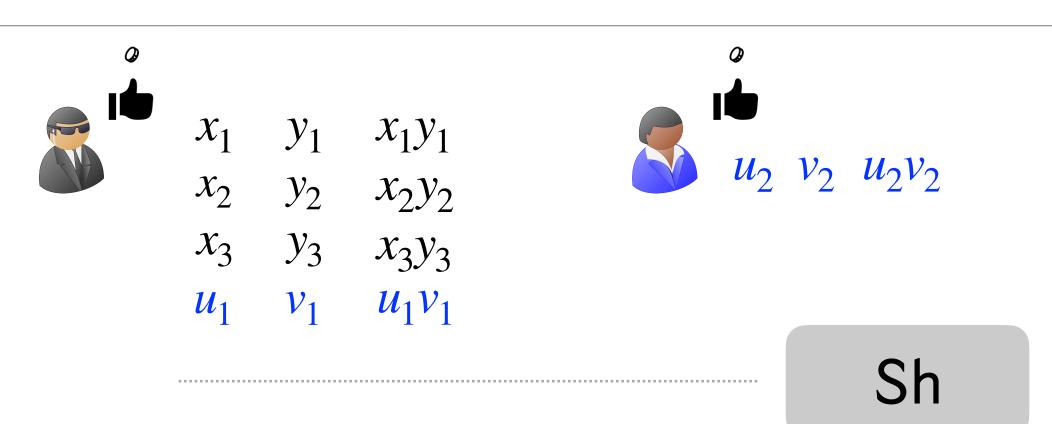


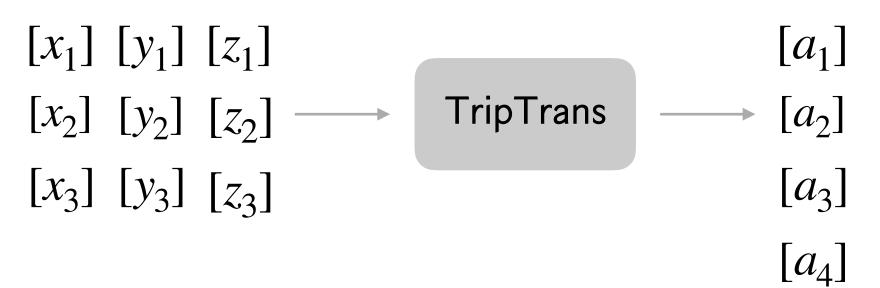


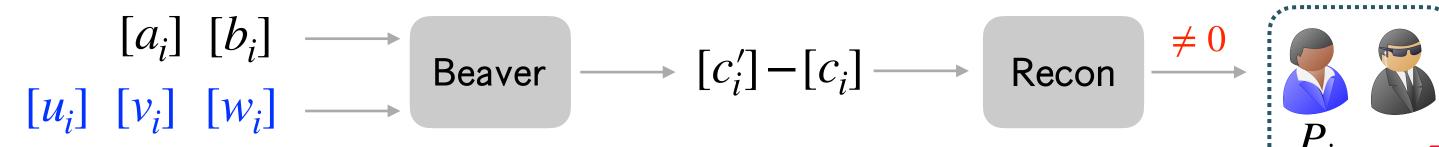


 $[a_1] [b_1] [c_1]$

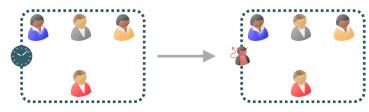
- $[a_4] [b_4] [c_4]$
- $[u_1] [v_1] [w_1]$ $[u_2] [v_2] [w_2]$ $[a_3] [b_3] [c_3] [u_3] [v_3] [w_3]$ $[u_4] [v_4] [w_4]$

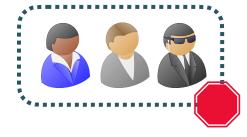




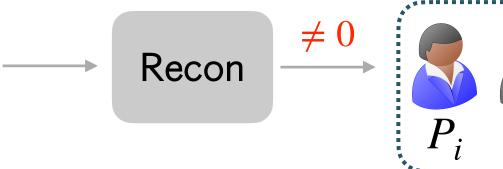


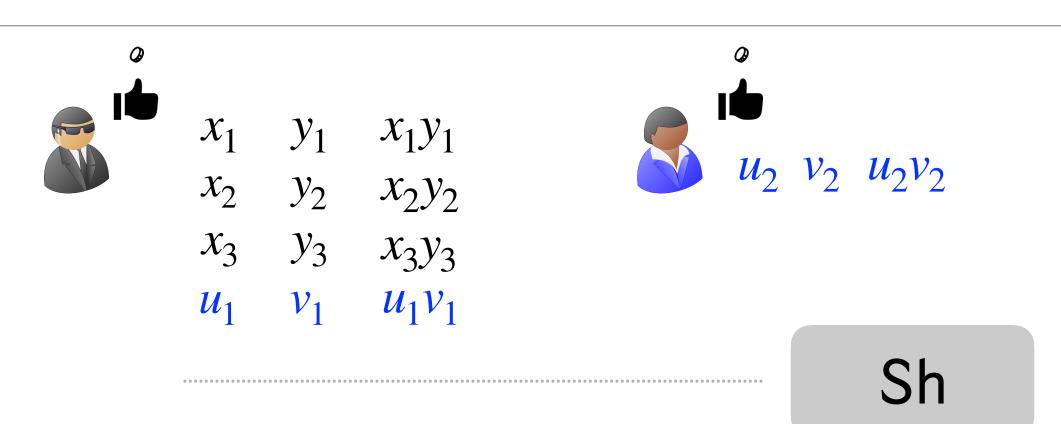


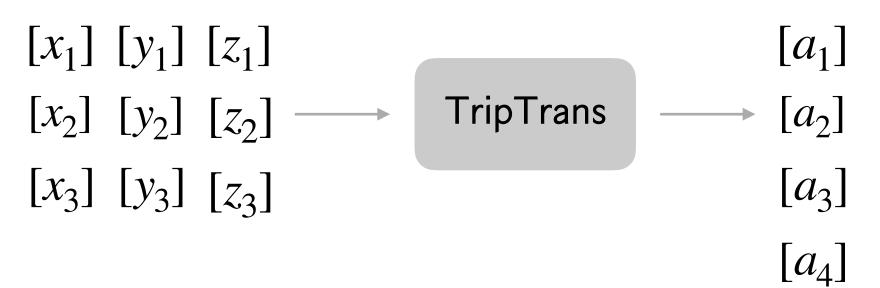


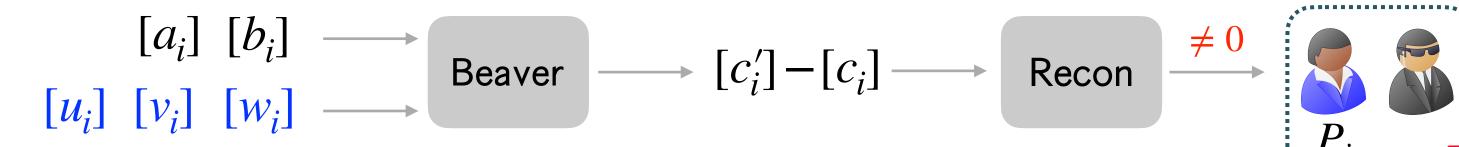


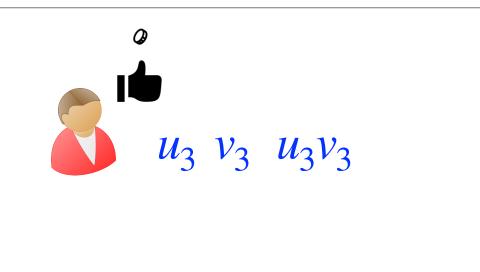
- $[a_1] [b_1] [c_1]$ $[a_2] [b_2] [c_2]$
- $[a_4] [b_4] [c_4]$
- $[u_1] [v_1] [w_1]$ $[u_2] [v_2] [w_2]$ $[a_3] [b_3] [c_3] [u_3] [v_3] [w_3]$ $[u_4] [v_4] [w_4]$

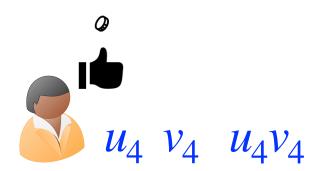


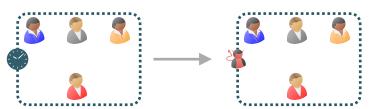










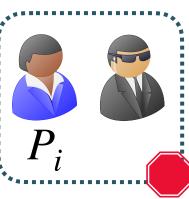




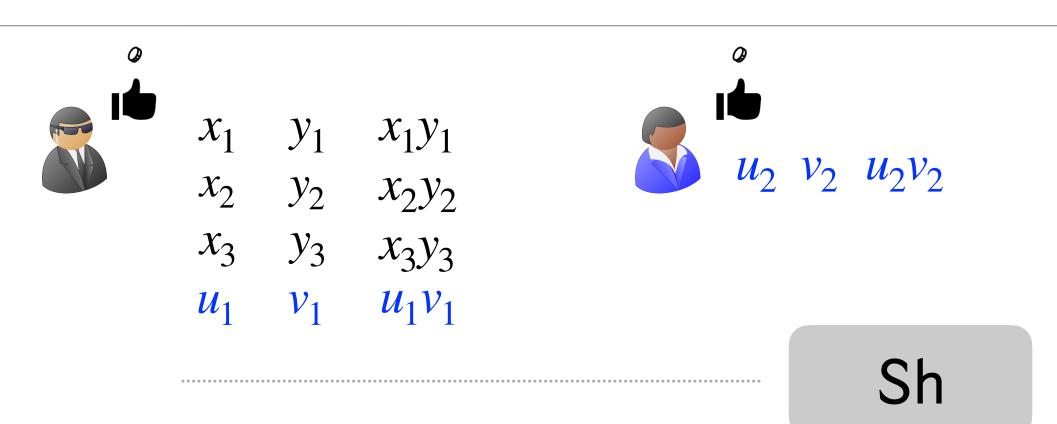
 $[a_1] [b_1] [c_1]$ $[b_2] [c_2]$ $[a_3] [b_3] [c_3]$

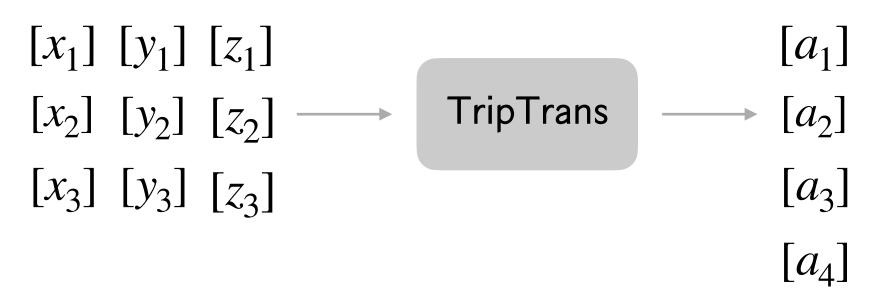
 $[a_4] [b_4] [c_4]$

 $[u_1] [v_1] [w_1]$ $[u_2] [v_2] [w_2]$ $[u_3] [v_3] [w_3]$ $[u_4] [v_4] [w_4]$

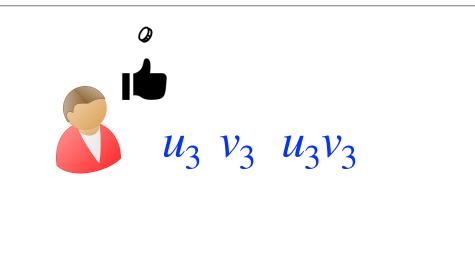


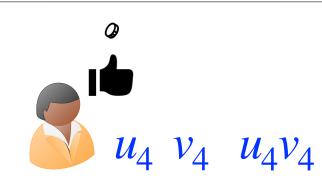
 $f_c(.) = f_a(.)f_b(.)$ if all checks hold

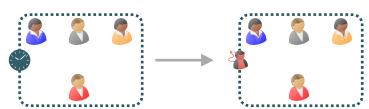








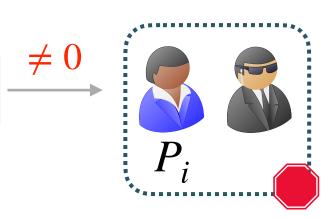


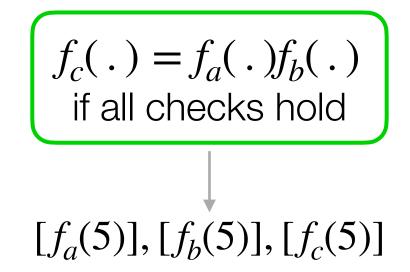




 $[a_1] [b_1] [c_1]$ $[b_2] [c_2]$ $[a_3] [b_3] [c_3]$ $[a_4] [b_4] [c_4]$

 $[u_1] [v_1] [w_1]$ $[u_2] [v_2] [w_2]$ $[u_3] [v_3] [w_3]$ $[u_4] [v_4] [w_4]$



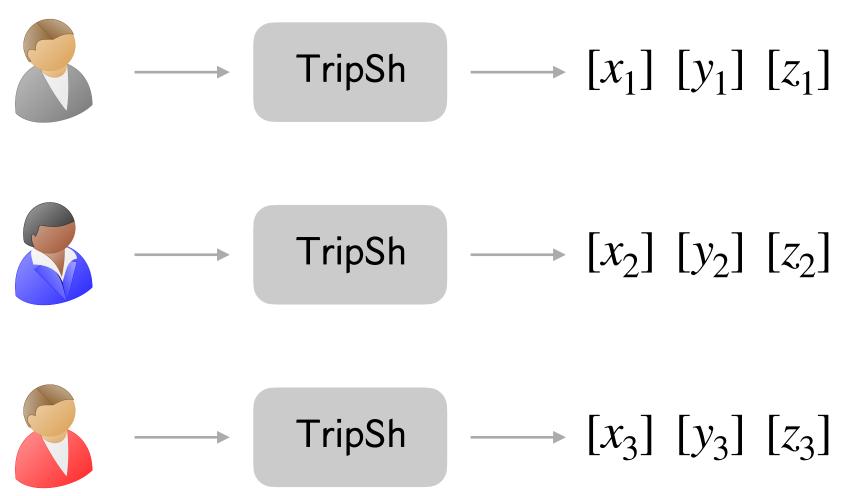


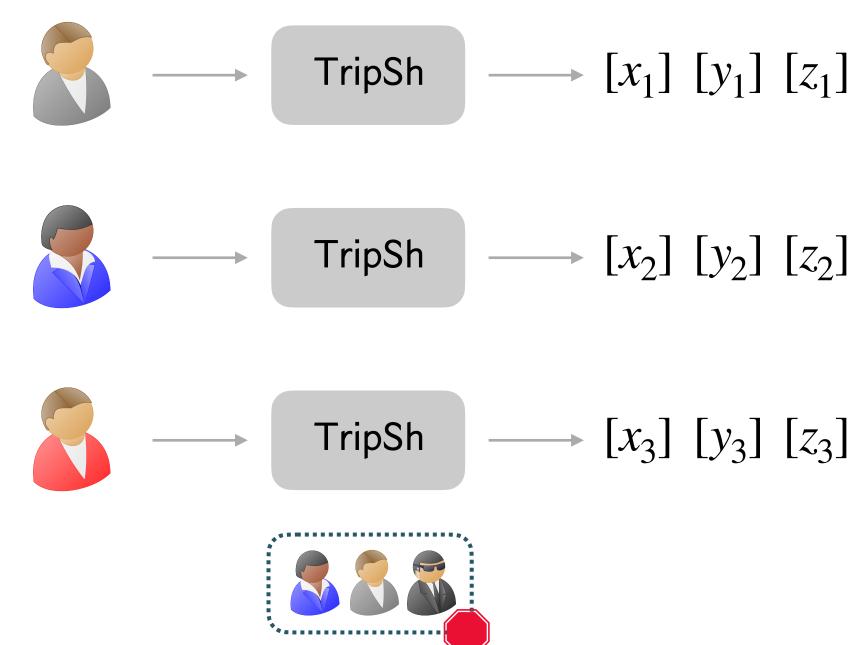


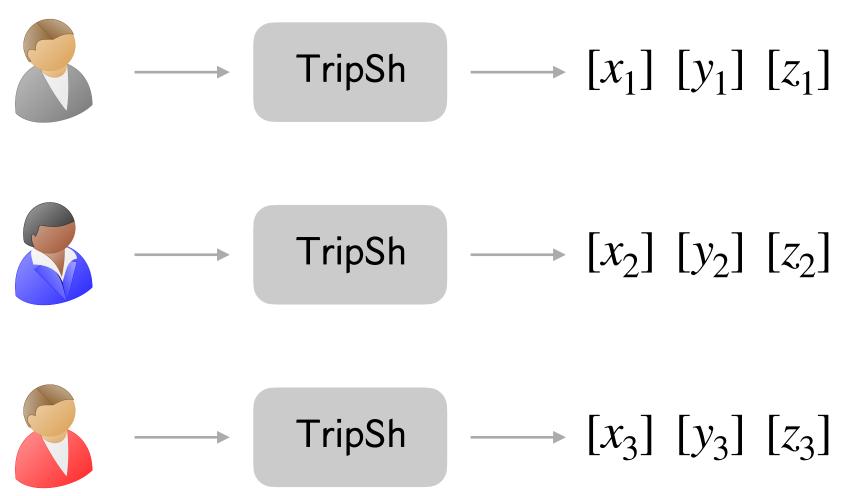


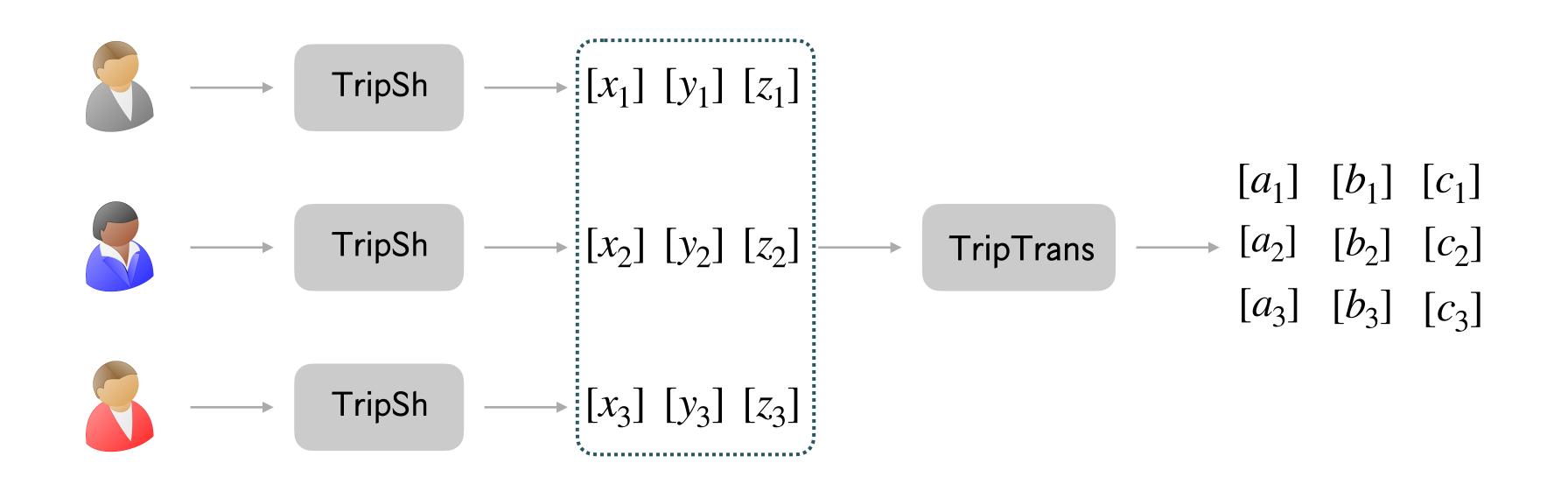


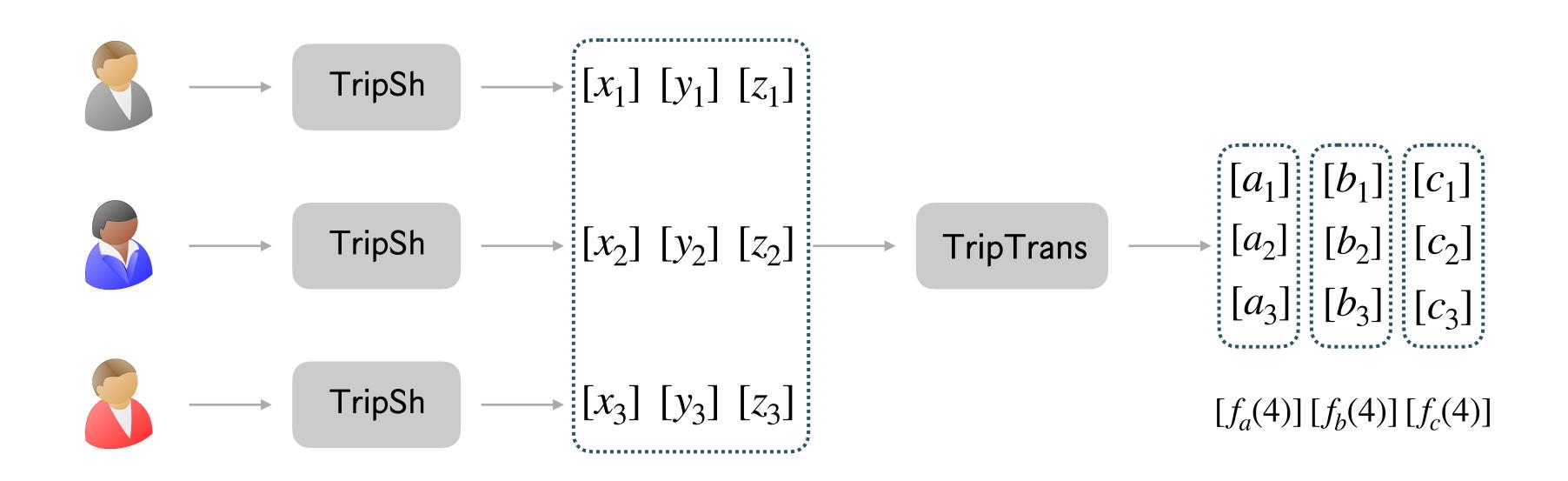


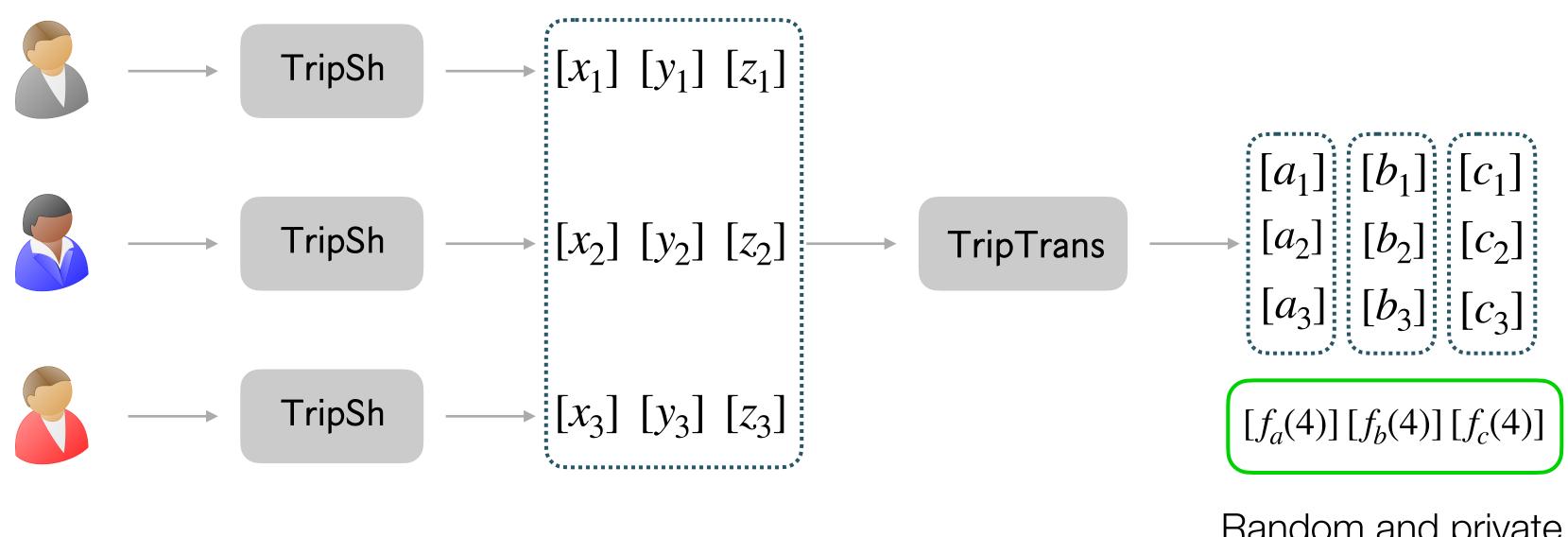






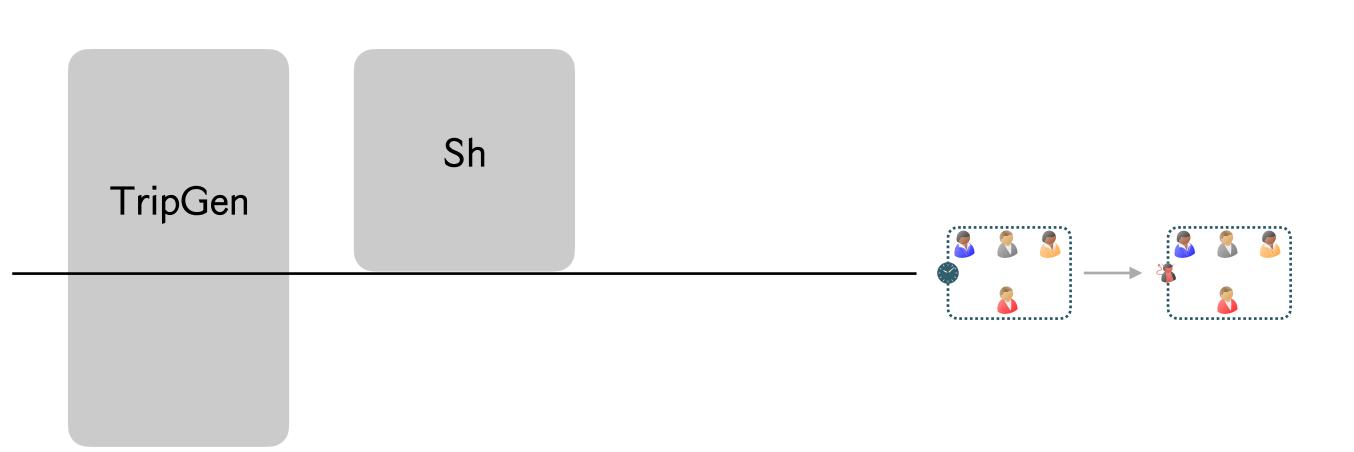






Random and private multiplication triple.

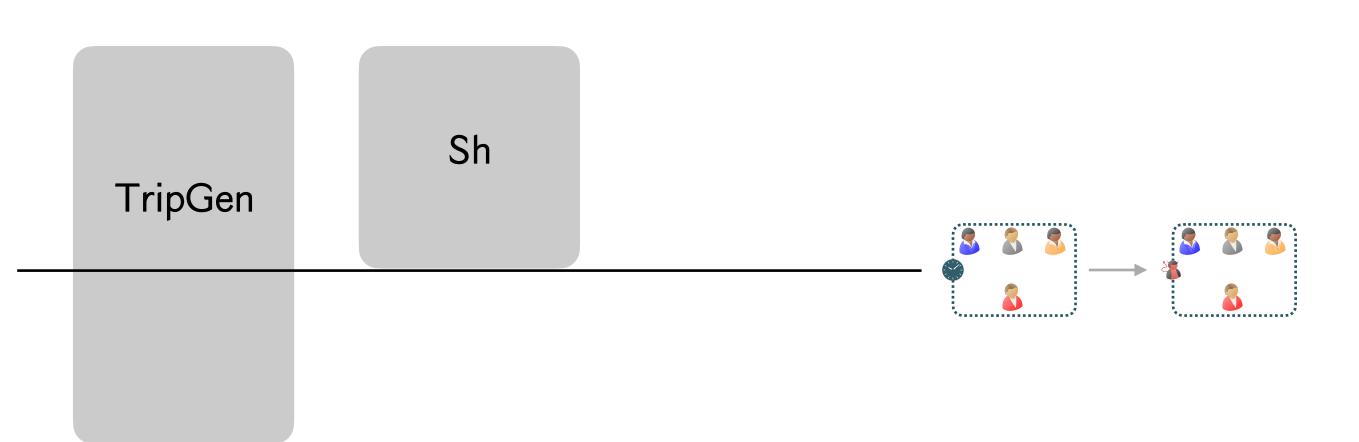
- 3 phases
 - Triple generation phase
 - Input phase
 - Circuit evaluation and output phase



Circuit Evaluation

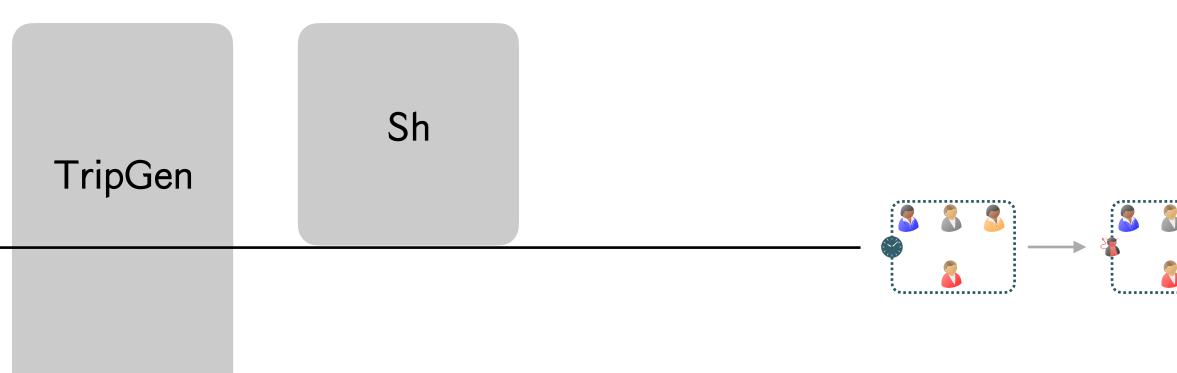
- Addition: Local
- Multiplication: **Beaver**
- Output: Recon

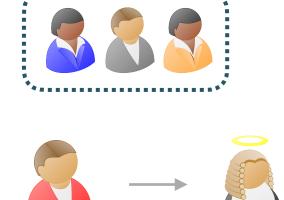
- 3 phases
 - Triple generation phase
 - Input phase
 - Circuit evaluation and output phase





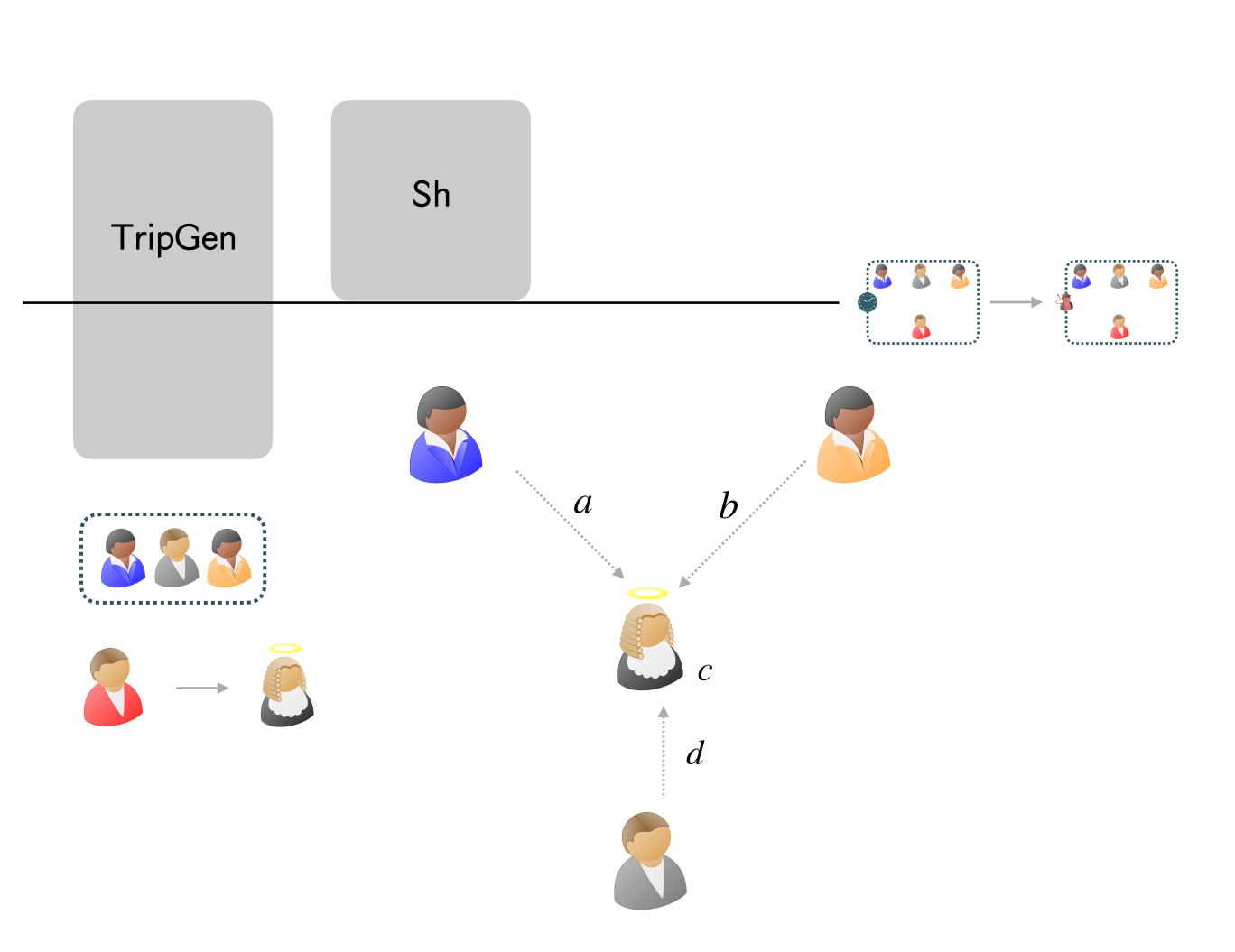
- 3 phases
 - Triple generation phase
 - Input phase
 - Circuit evaluation and output phase



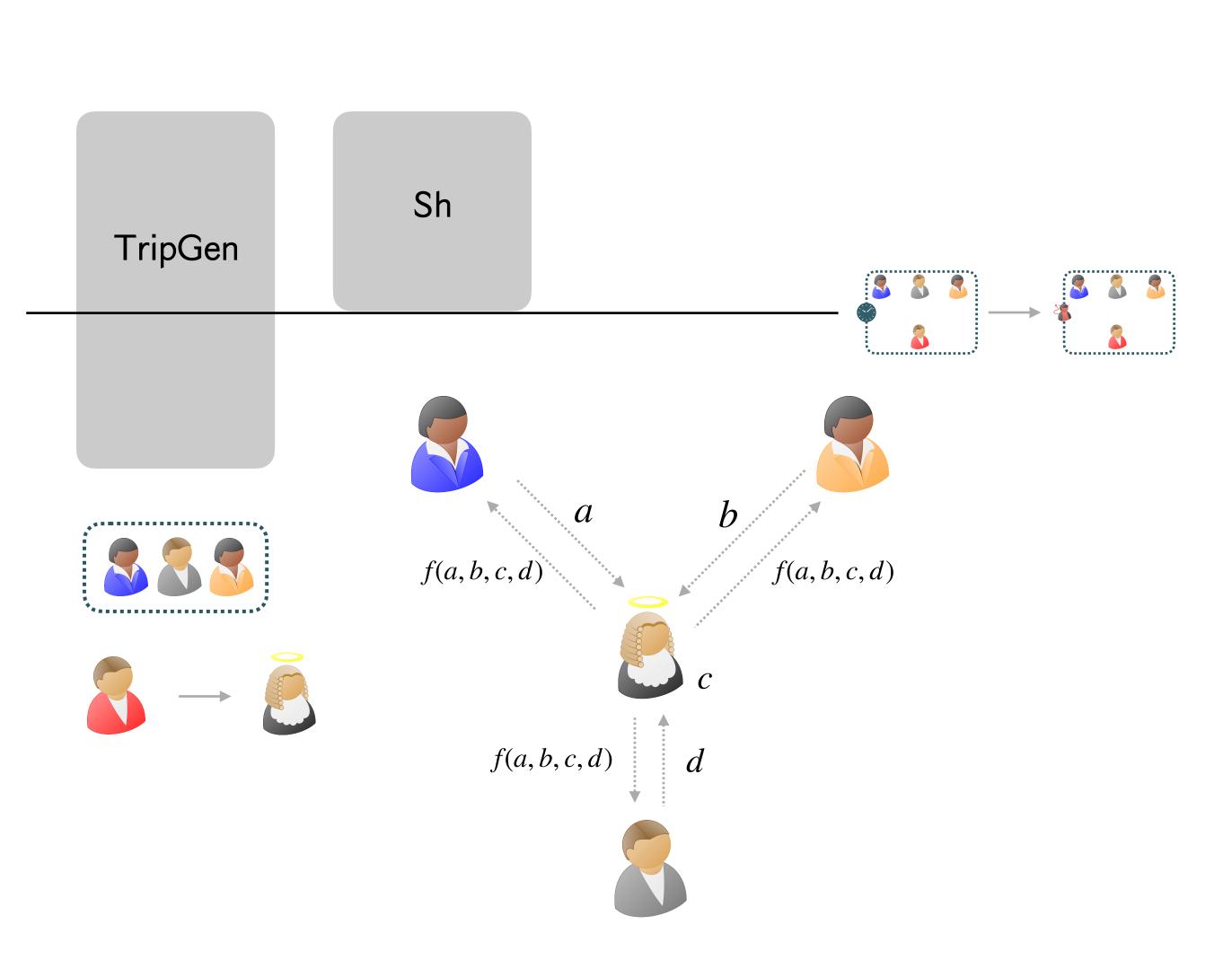




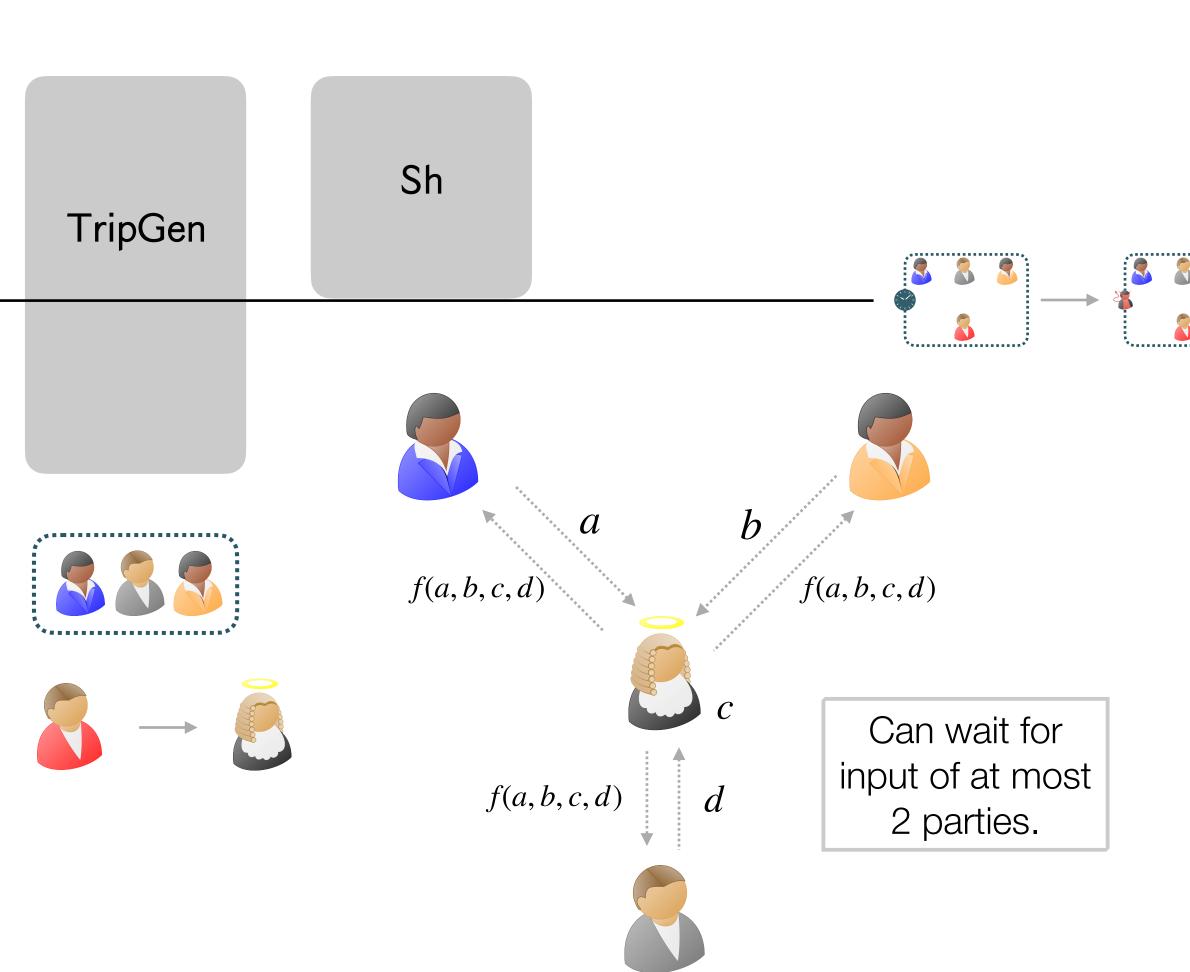
- 3 phases
 - Triple generation phase
 - Input phase
 - Circuit evaluation and output phase



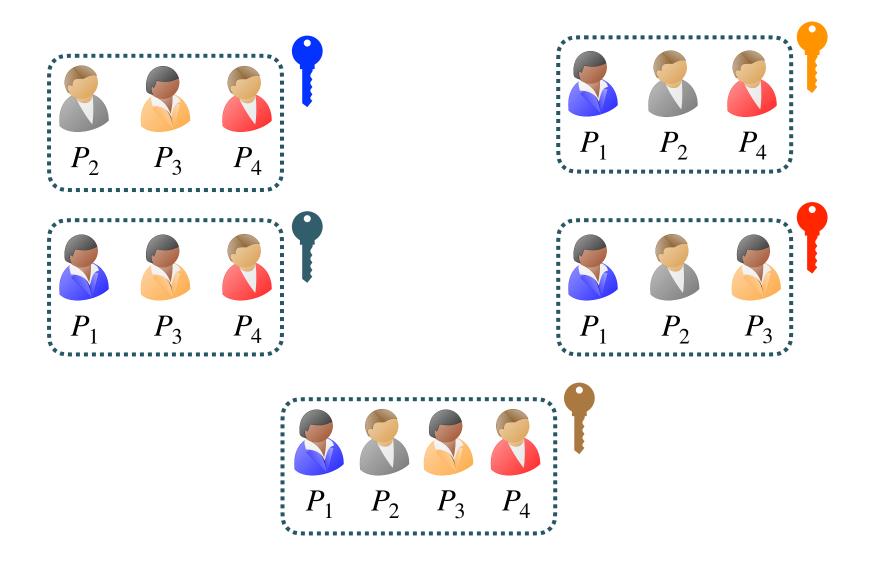
- 3 phases
 - Triple generation phase
 - Input phase
 - Circuit evaluation and output phase



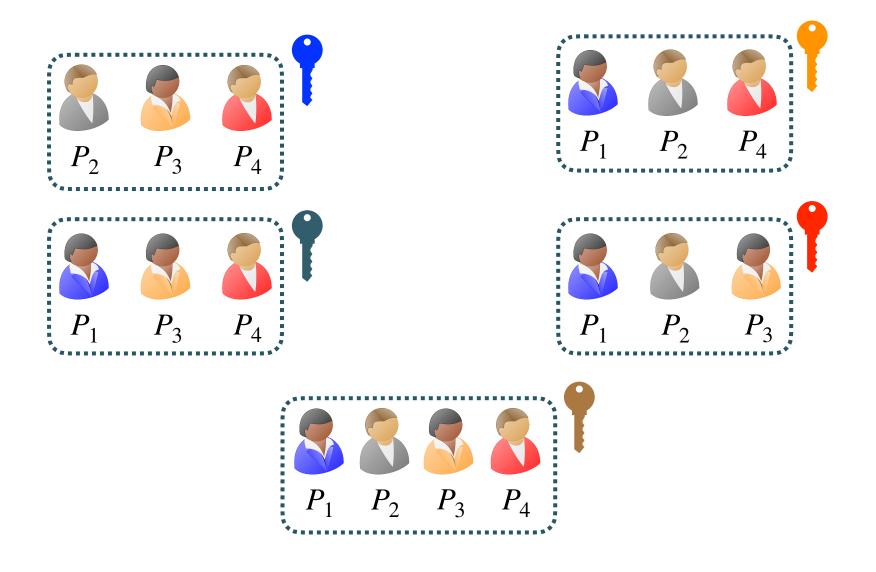
- 3 phases
 - Triple generation phase
 - Input phase
 - Circuit evaluation and output phase





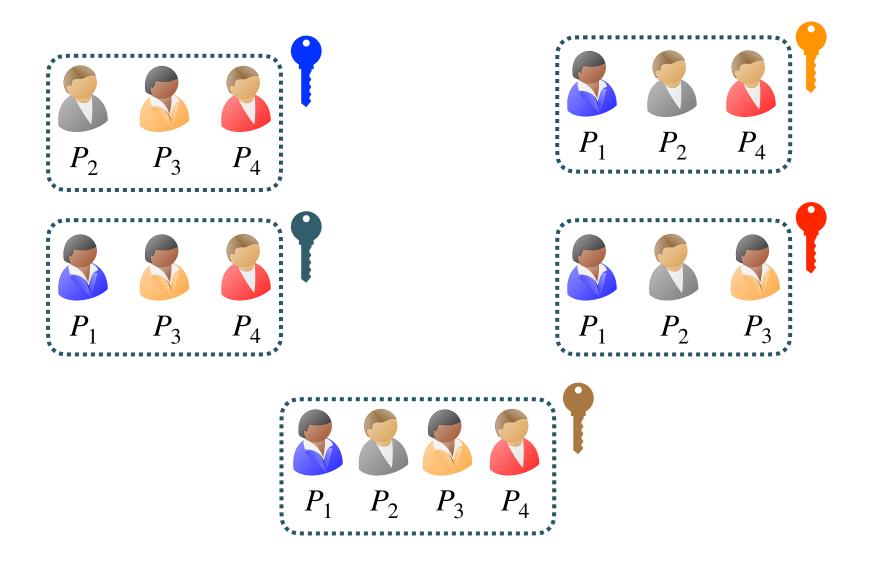


Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •

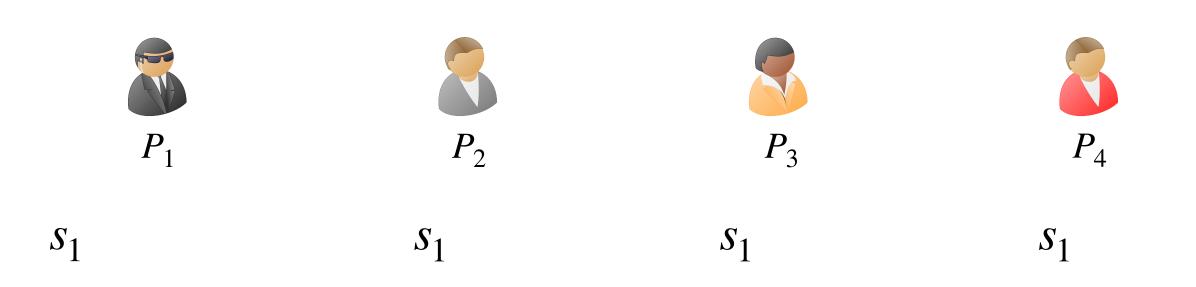


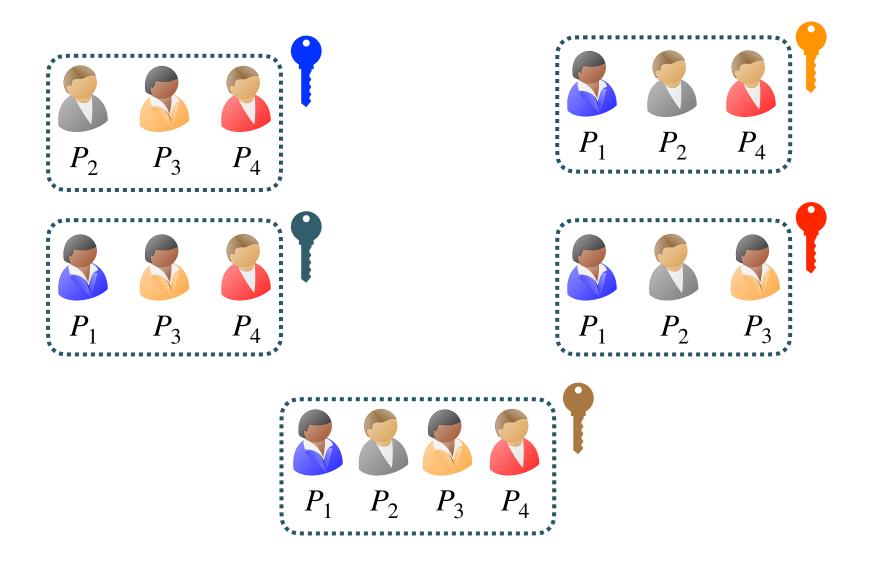
- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol



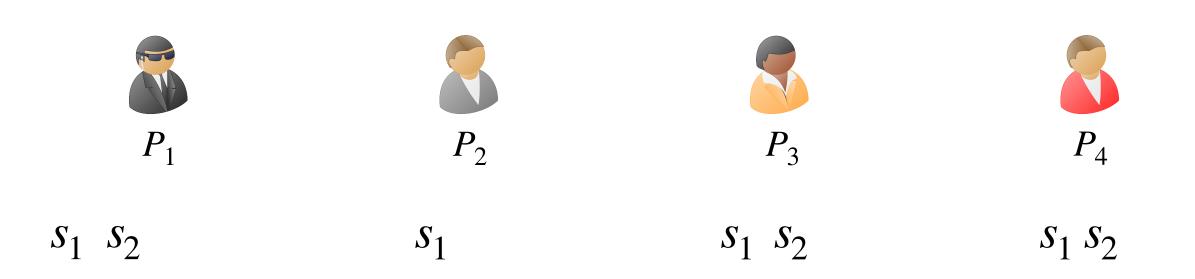


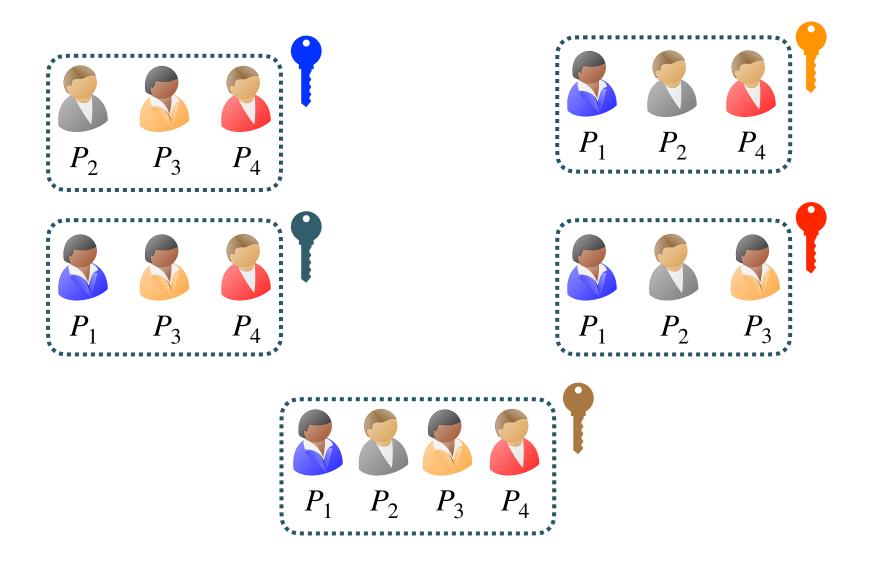
- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol





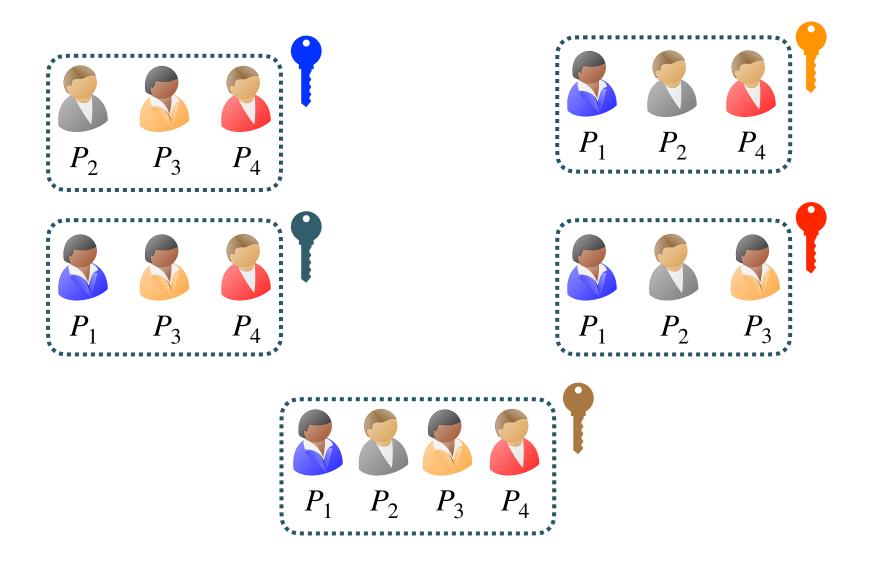
- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol



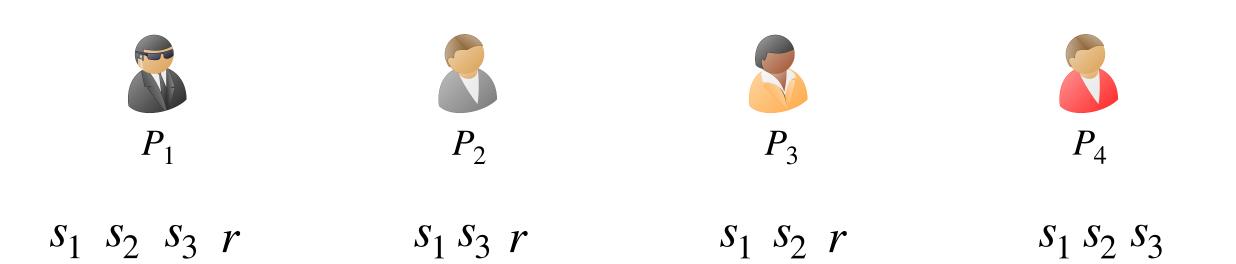


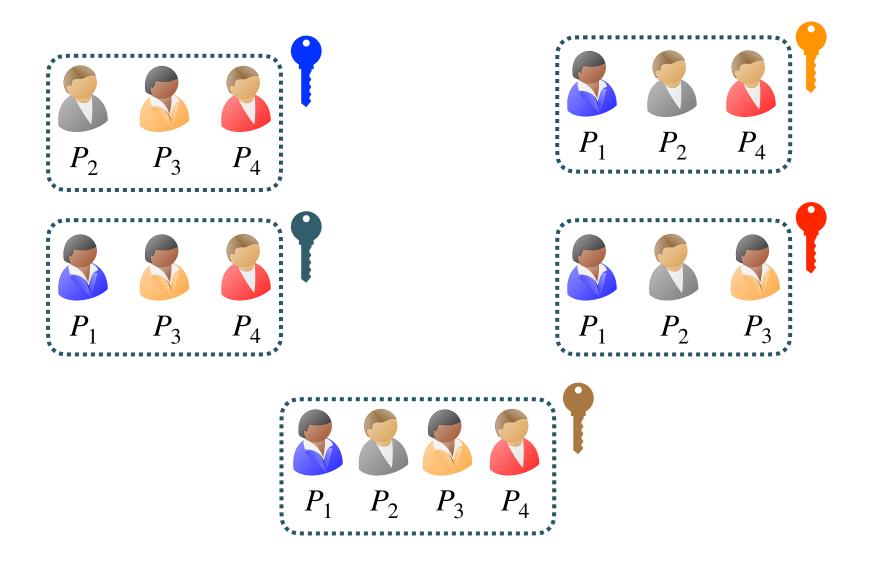
- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol



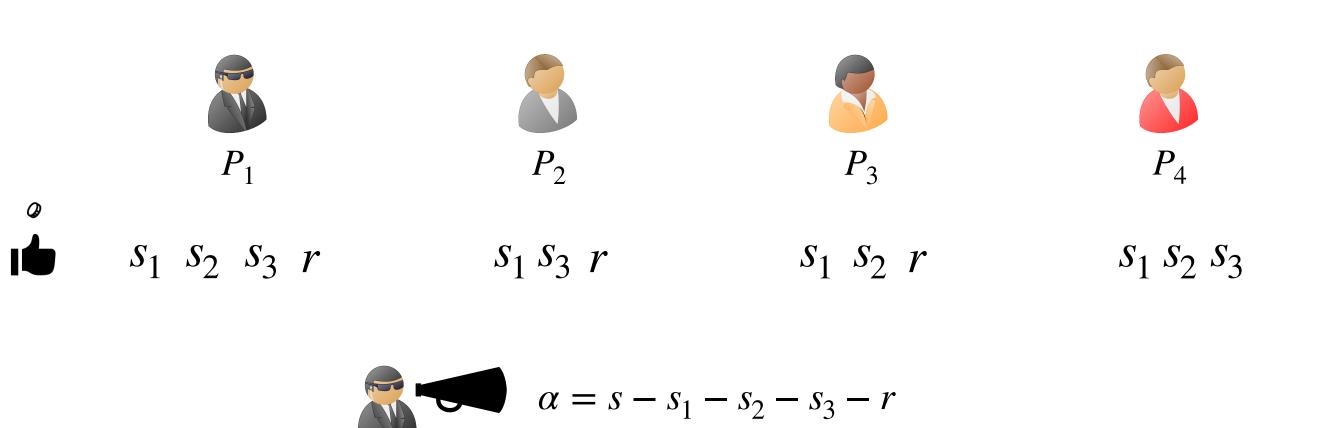


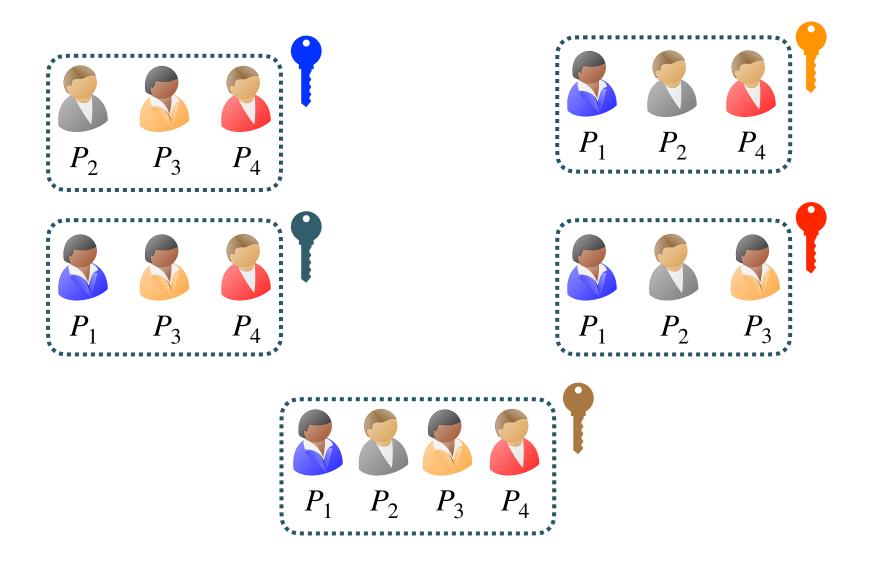
- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol



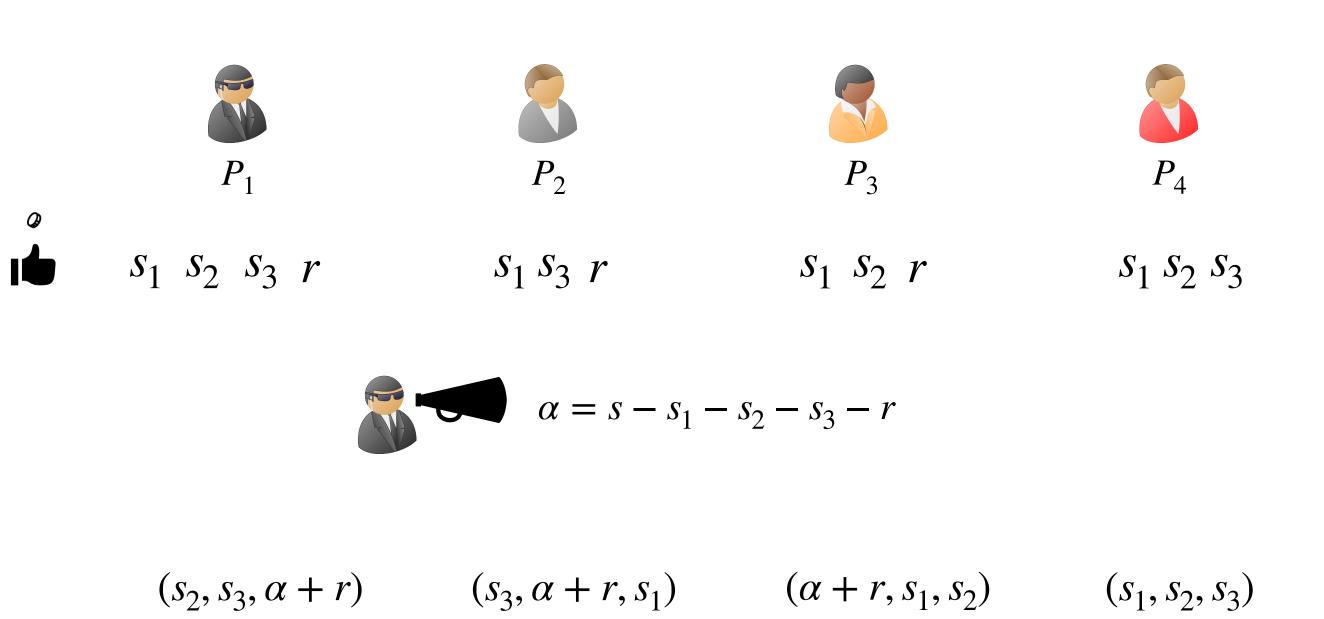


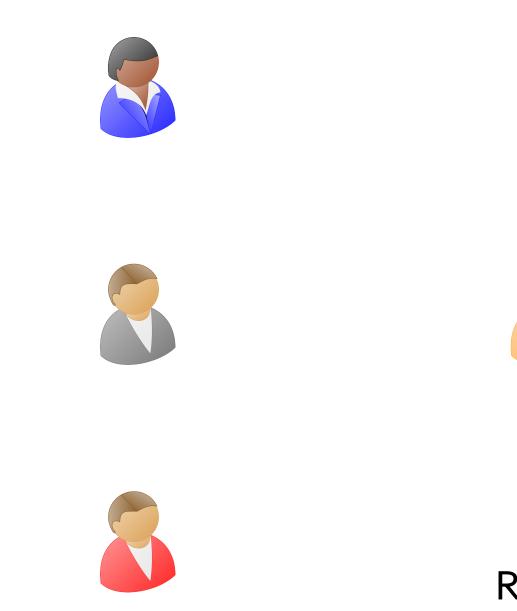
- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol





- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol

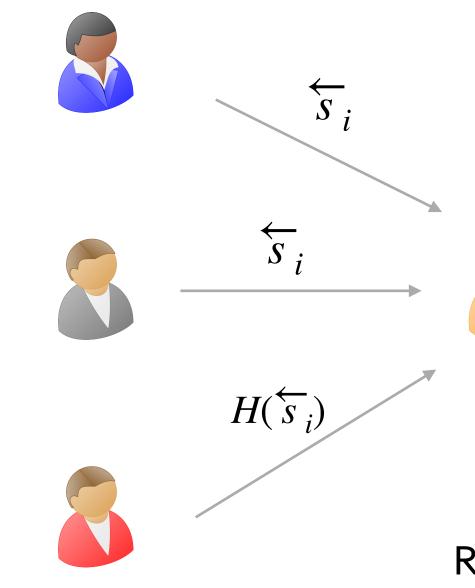




- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol •
- Efficient reconstruction protocol •



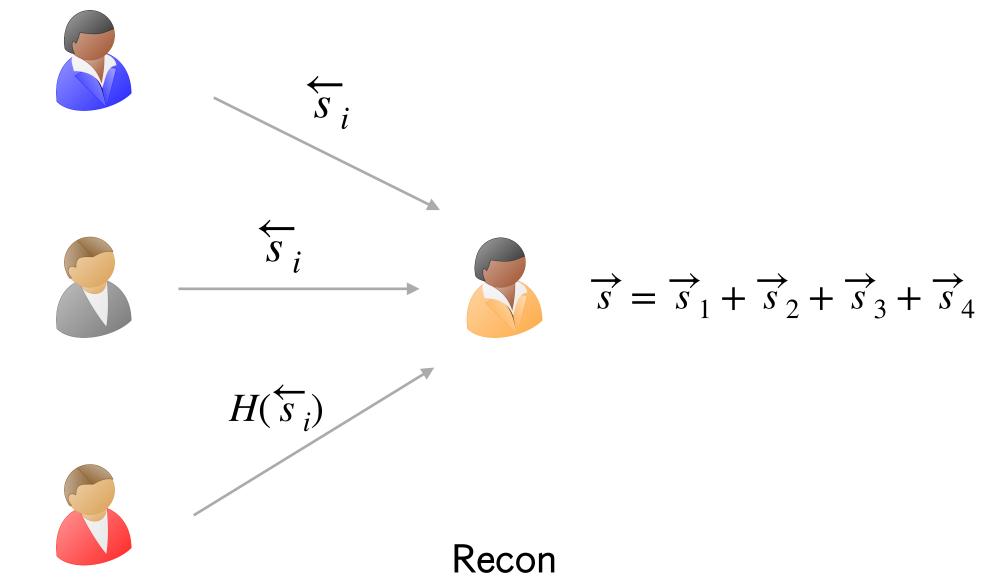
Recon



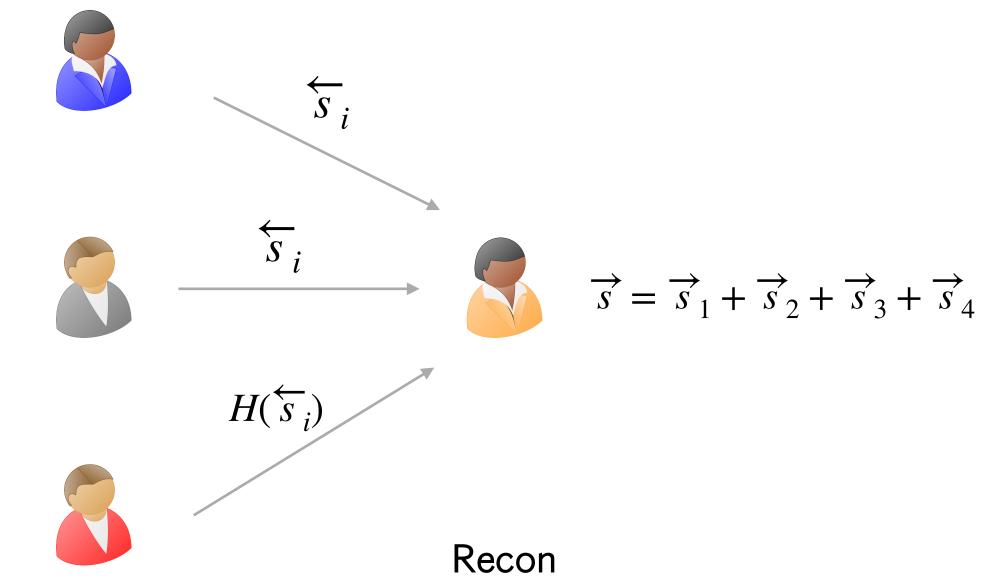
- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol •
- Efficient reconstruction protocol •



Recon



- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol •
- Efficient reconstruction protocol •



- Assume symmetric-key setup for PRF [AFL+16,CCP+19,MR18] •
 - One synchronous round VSS protocol •
- Efficient reconstruction protocol •

Completely Asynchronous

- Triple sharing similar to TripSh
 - Dealer shares 2l + 1 triples instead of 3 triples
 - Other parties don't share triples

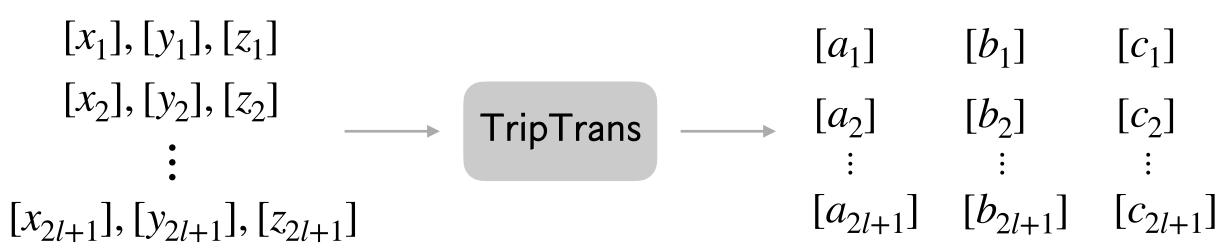
- Triple sharing similar to TripSh •
 - Dealer shares 2l + 1 triples instead of 3 triples

 Other parties don't share triples

 $[x_1], [y_1], [z_1]$ $[x_2], [y_2], [z_2]$ $[x_{2l+1}], [y_{2l+1}], [z_{2l+1}]$

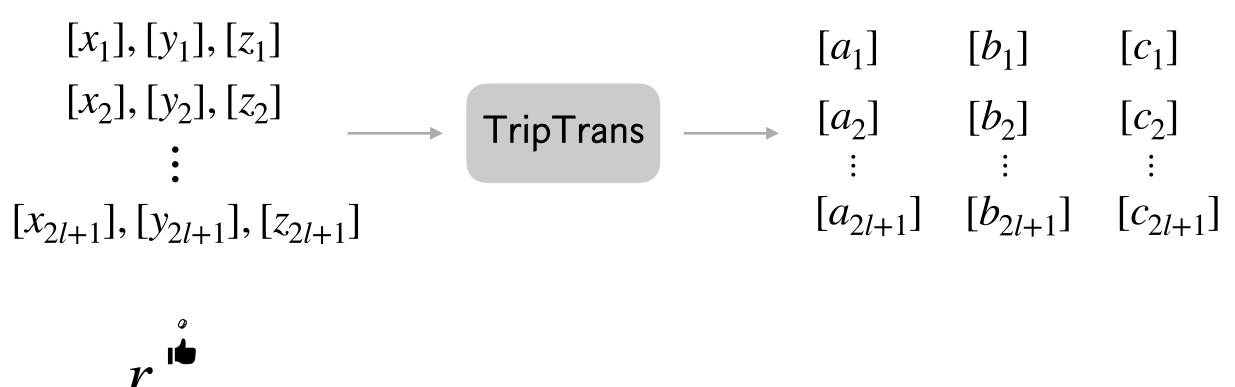
- Triple sharing similar to **TripSh** •
 - Dealer shares 2l + 1 triples instead of 3 triples

Other parties don't share • triples

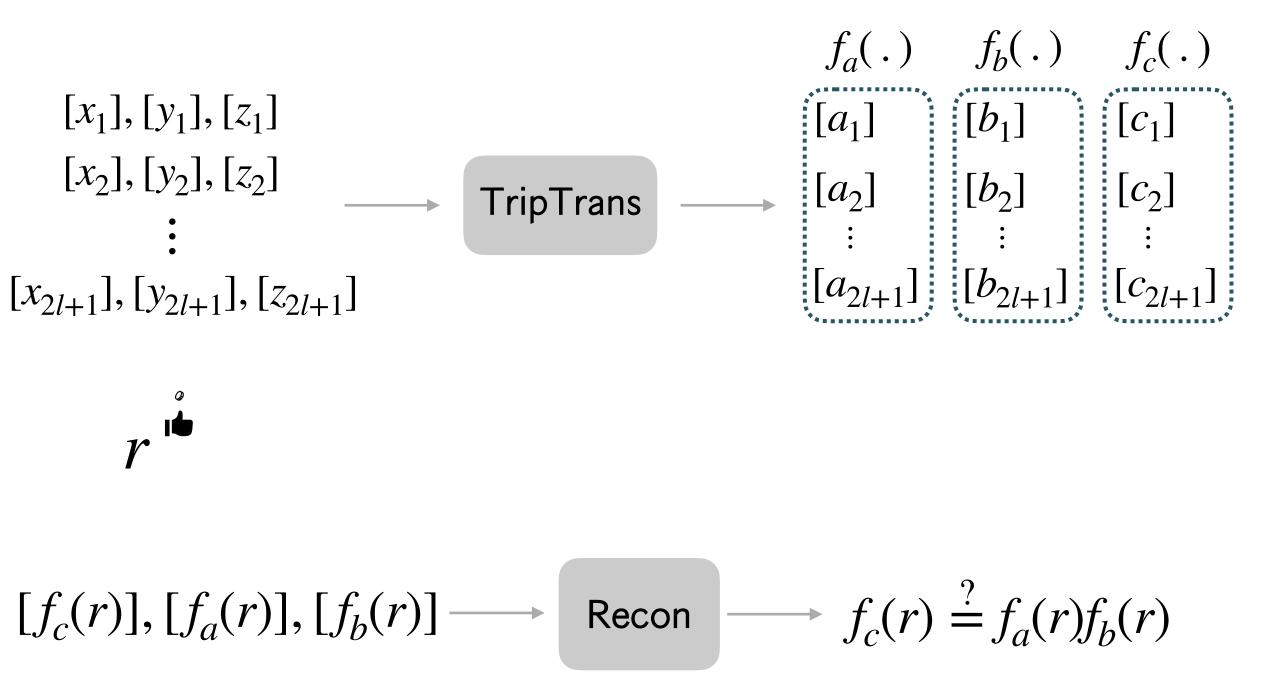


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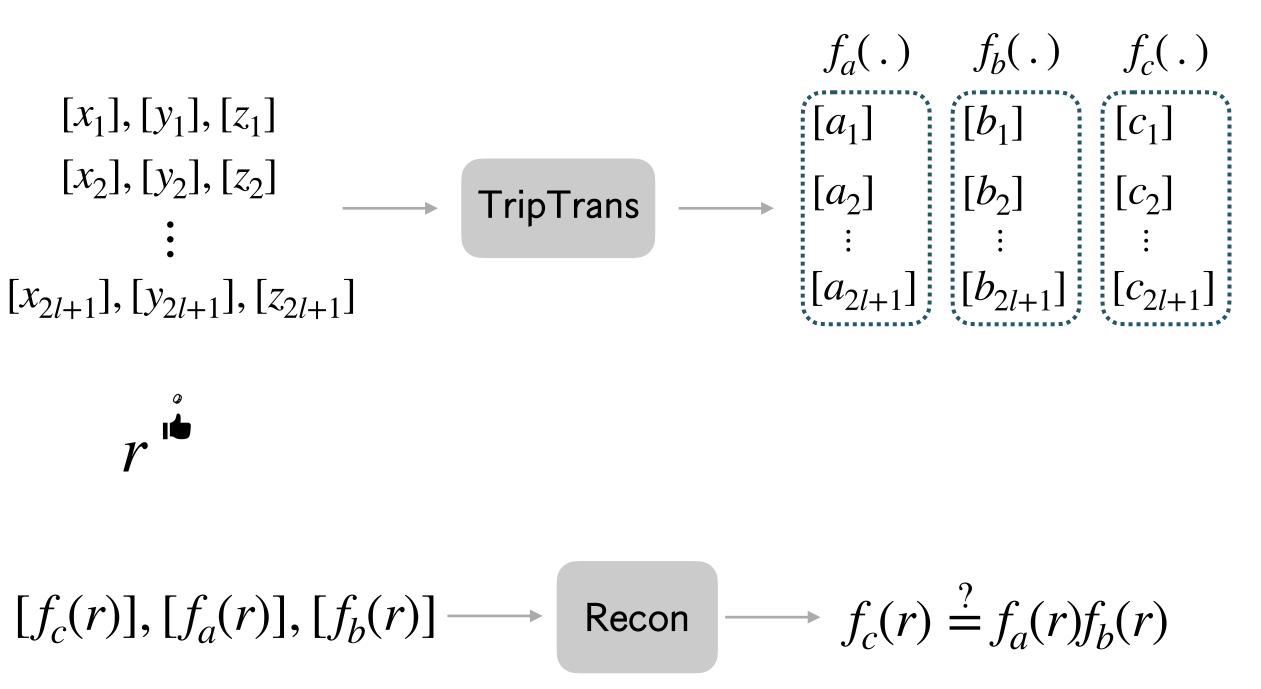
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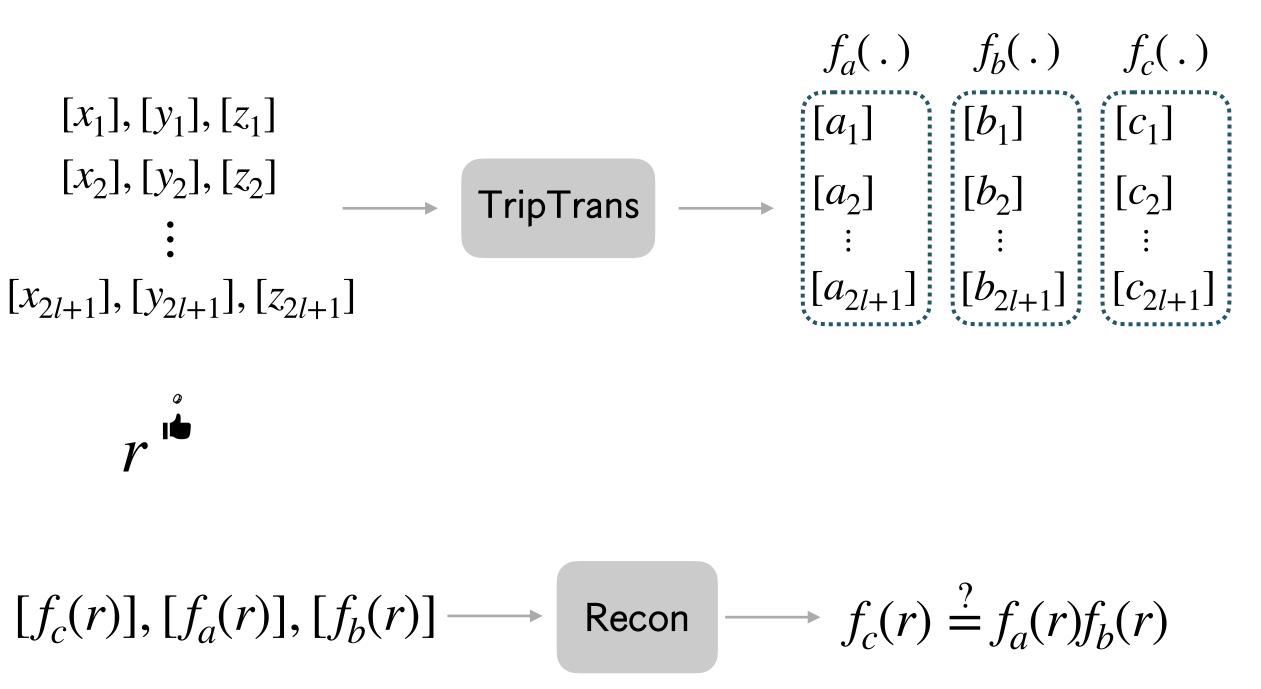


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l multiplication triples *l* shares of ([0], [0], [0])

- Triple sharing similar to TripSh
 - Dealer shares 2l + 1 triples instead of 3 triples
 - Other parties don't share triples
- Triple generation similar to
 TripGen
 - Each instance outputs *l* triples



l multiplication triples *l* shares of ([0], [0], [0])

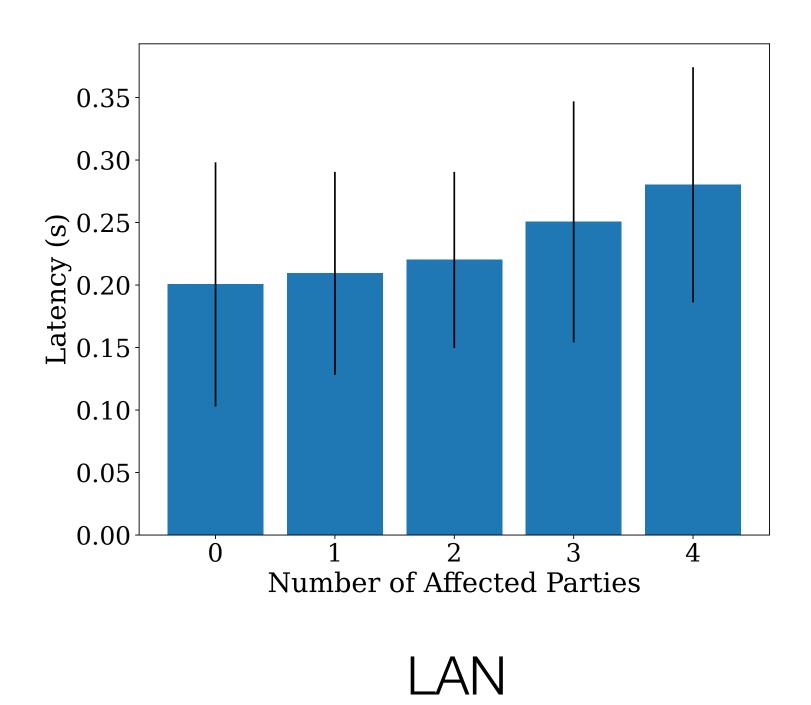
Cryptographically Secure HMPC and AMPC

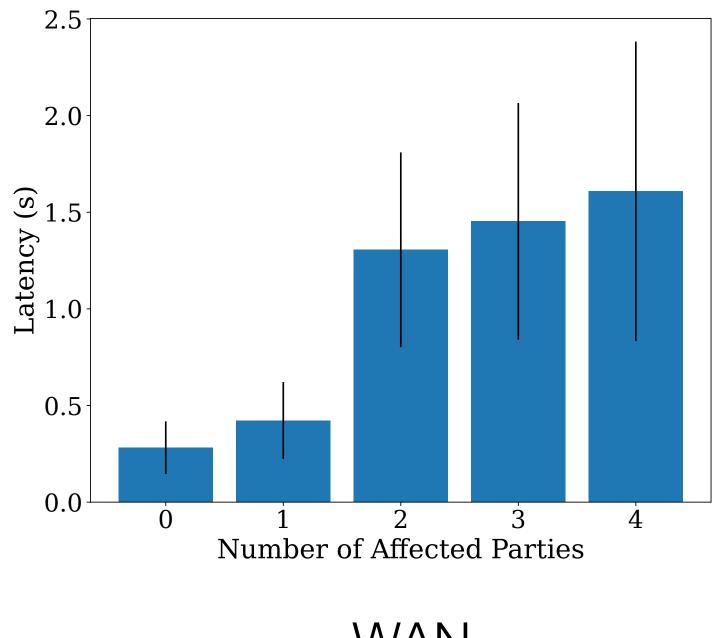
- Cryptographically secure HMPC •
 - Triple generation phase and input phase use 1 synchronous round
 - Circuit evaluation is completely asynchronous
 - Input provision •

Cryptographically Secure HMPC and AMPC

- Cryptographically secure HMPC •
 - Triple generation phase and input phase use 1 synchronous round
 - Circuit evaluation is completely asynchronous
 - Input provision •
- Cryptographically secure AMPC •
 - Similar to Cryptographically secure HMPC
 - No synchronous broadcast \implies ACast and ACS •
 - No input provision

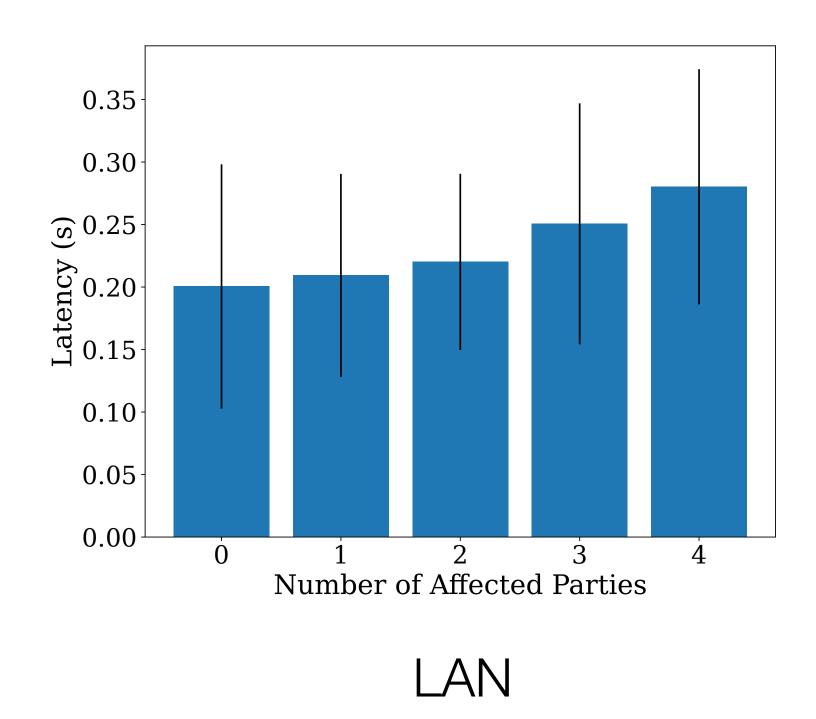
Conclusion



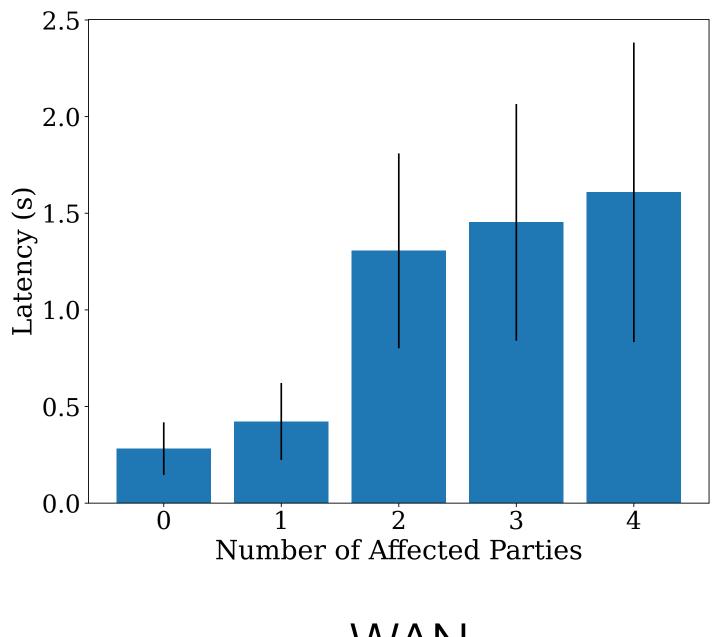


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Conclusion



- Open problems •
 - Perfect HMPC protocol for general case •
 - Bridging the gap between synchronous and asynchronous MPC protocols •



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Thank You

